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EXAMINER	
PATEL, HARESH N	

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/881,367
Filing Date: June 14, 2001
Appellant(s): JHA, PANKAI K.

Mr. John J. Ignatowski
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 3/9/2006 appealing from the Office action mailed 5/3/2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The brief does not contain a statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief. Therefore, it is presumed that there are none. The Board, however, may exercise its discretion to require an explicit statement as to the existence of any related appeals and interferences.

The Examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct. Note: the claim 18 is objected in final office action dated 5/3/2005.

(4) Status of Amendments After Final

The Appellant's statement of the status of amendments after final rejection contained in the brief is correct. (Note: An advisory action dated 6/28/2005 was issued regarding the Appellant's proposed amending the rejected claimed subject matter, with additional limitations, "from a database storing", " into said database", "protocol from a database", "delineate said receive frame", "protocols to frame said outgoing packets", "packet generated from said second incoming packet", "a database configured", "peripheral means", "configured to perform a different operation", after final office action dated 5/3/2005 was issued. The pre-appeal

conference, dated 10/20/2005, containing notice of panel decision from Pre-appeal Brief Review sustained the rejections of the claims 1-20, please see Pre-Appeal conference decision dated 10/20/2005).

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

Note: The summary of the claimed subject matter, page 2, line 2- page 5, line 3, of the appeal brief, dated 3/9/2006 contains very specific details regarding the broadly claimed subject matter of the claims (please refer to claims on appeal, pages 39-43, of the appeal brief, dated 11/21/2005).

The summary of the claimed subject matter, page 2, line 2- page 5, line 3, of the appeal brief, dated 3/9/2006, contains very specific details regarding claim 1 as following:

1) an Ethernet frame
2) signal POINTER
3) MAC destination, MAC source, PDI
4) reading the first parameter off the incoming packet
5) Once the parameter is found ...
6) reading implemented by a parser circuit
7) matching address (contrary to producing parameter of the claim 1)
8) processing implemented by a number of peripherals
9) assembling the parameter
10) framing an outgoing frame
11) then transmitting the outgoing frame, and
12) presenting implemented by an assembler circuit, which is **not what the claimed invention i.e., claimed subject matter of the claim 1 reflect and limited to** (please see claim 1).

The summary of the claimed subject matter, page 2, line 2- page 5, line 3, of the appeal brief, dated 3/9/2006, contains very specific details regarding claim 16 as following:

1) an Ethernet frame
2) signal POINTER
3) MAC destination, MAC source, PDI

which is **not what the claimed invention i.e., claimed subject matter of the claim 16 reflect and limited to** (please see claim 16, including the limitations supporting "means for").

Note: The dependent claims include the claimed subject matter of their respective independent claims.

(6) Grounds of Rejection to be Reviewed on Appeal

The Appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Grouping of Claims

The rejection of claims 1-20 stand or fall together because Appellant's brief does not include a statement that this grouping of claims do not stand or fall together and reasons in support thereof. See 37 CFR 1.192(c)(7).

(9) Evidence Relied Upon

5,936,966	Ogawa et. al.	8-1999
5,633,806	Yusa et. al.	5-1997
6,687,247	Wilford et. al.	2-2004

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Double Patenting

Appellant's submission of terminal disclosure to overcome double patenting rejection with **copending application** 09/881,493, dated 11/26/2004 has been acknowledged. Note: Even

though the terminal disclosure is filled, **none of the claims of the copending application has been allowable** or **allowed** or **patentable** and is still under prosecution.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-8, 10-17 are rejected under 35 U.S.C. 1O2(e) as being anticipated by Ogawa et al. 5,936,966 (Hereinafter Ogawa).

As per claims 1 and 16, Ogawa teaches a method (e.g., col., 3, lines 44 – 59) / a circuit (e.g., col., 6, lines 56 – 67) for bridging (e.g., col., 5, lines 11 – 15) an incoming packet (e.g., col., 4, line 65 – col., 5, line 6) from a first network to a second network (e.g., another network, col., 5, lines 11 – 15, e.g., use of internetwork repeater between first and second networks, col., 12, lines 41 – 49, col., 2, lines 5 – 14) comprising:

reading a pointer (e.g., col., 13, lines 50 –55) for a first parameter (e.g., parameter of the received frame, col., 11, lines 58 – 67, col., 13, lines 15 – 21) within an incoming packet (e.g., col., 12, lines 53 – 63, figure 5) complaint with a network protocol (e.g., col., 7, lines 54 - 58),

processing the first parameter (e.g., col., 13, lines 15 – 21) in accordance with the pointer (e.g., col., 13, lines 50 –55) to produce a second parameter (e.g., col., 9, lines 7 – 24), and

presenting an outgoing packet (e.g., col., 8, lines 50 – 63) containing said second parameter (e.g., col., 9, lines 7 – 24) for said second network (e.g., col., 5, lines 11 – 15, col., 12, lines 41 – 49, col., 2, lines 5 – 14).

As per claims 2 and 17, Ogawa teaches the following:

reading a length and an offset for said first parameter (e.g., parameter of the received frame, col., 11, lines 58 – 67, lines 27 - 65, col., 9),

partitioning said incoming packet in accordance with said offset and said length to extract said first parameter prior to processing (e.g., lines 27 - 65, col., 9).

As per claim 3, Ogawa teaches the following:

downloading said offset, said length, and said pointer prior to reading (e.g., lines 27 - 65, col, 9).

As per claim 4, Ogawa teaches the following:

routing said first parameter a peripheral block identified by said pointer prior to processing (e.g., col., 3, lines 44 - 65), wherein said peripheral blocks perform said processing (e.g., lines 44 - 60, col., 4) and

assembling said second parameter into said outgoing packet in response to processing (e.g., line 54, col., 7 - line 12, col., 8).

As per claim 5, Ogawa teaches the following:

reading second offset and a second length for second network protocol prior to assembling said outgoing packet (e.g., lines 19 - 67, page 10).

As per claim 6, Ogawa teaches the following:

routing said first parameter to an external peripheral block identified by said pointer prior to processing (e.g., col., 3, lines 44 - 65), wherein said external peripheral block performing said processing (e.g., line 54, col., 7 - line 12, col., 8).

As per claim 7, Ogawa teaches the following:

at least two processes a content addressable memory process, a time to live process, comparison process, counter process, a value swapping process, a stuffing process, cyclic redundancy a de-stuffing process, checksum process, a parity process, a first-in- first-out process, a length construction generator header error control synchronization process, a frame relay lookup process, data link connection identifier process, protocol identification analysis process, point-to-point protocol verification process, parameter discard process, and a buffer process (e.g., col., 3, line 60 – col., 4, line 11).

As per claim 8, Ogawa teaches the following:

step (B) comprises the sub-step of simultaneously processing a plurality of parameters within said incoming packet (e.g., col., 4, lines 13 - 31).

As per claim 10, Ogawa teaches the following:

delineating a receive produce frame from said first network to produce said incoming packet prior to processing said incoming packet prior to processing (e.g., lines 44 - 60, col., 4).

As per claim 11, Ogawa teaches the following:

selecting among plurality of frame delineation plurality of network protocols prior to delineating (e.g., line 54, col., 7 - line 12, col., 8).

As per claim 12, Ogawa teaches the following:

delineating a second receive frame from said second network to produce said incoming packet (e.g., line 54, col., 7 - line 12, col., 8).

As per claim 13, Ogawa teaches the following:

framing said outgoing to produce a transmit frame for said second network in response to presenting said outgoing packet (e.g., col., 3, lines 44 - 65).

As per claim 14, Ogawa teaches the following:

selecting among a plurality of framing methods for a plurality of network protocols prior to framing (e.g., lines 21 - 36, col., 10).

As per claim 15, Ogawa teaches the following:

framing said output packet to produce a second transmit frame for said network in response presenting said outgoing packet (e.g., lines 2 - 24, col., 9).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ogawa in view of "Official Notice".

As per claim 9, Ogawa teaches the claimed limitation as rejected under claim 1. However, Ogawa does not specifically mention about step (B) being non-programmable. "Official Notice" is taken that both the concept and advantages of providing step (B) being non-programmable is well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the concept of making the processing non-programmable with the teaching's of Ogawa in order to facilitate non-programmable processing for the step (B). The concept of non-programmable processing would enhance processing the steps taught by the Ogawa. For example, Yusa et al., 5,633,806, discloses the well-known concept of non-programmable processing (e.g., use of fixed function in the core region, col., 14, lines 6 – 21). The usage of non-programmable circuit design would help increase the degree of freedom of circuit design.

Claims 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ogawa in view of Wilford et al., 6,687,247 (Hereinafter Wilford).

As per claim 18, Ogawa teaches the claimed limitation as rejected under claims 16 and 17. However, Ogawa does not specifically disclose a plurality of peripheral means at least one (i) linked to the pointer and (ii) configured to perform a process involving the first parameter.

Wilford discloses a plurality of peripheral means (e.g., use of modules of memory or memory controller that does processing, figures 9, 10, 15, 26) at least one (i) linked to the pointer (e.g., concept of TAG usage, col., 49, lines 15 – 38) and (ii) configured to perform a process (e.g., perform handling information, col., 6, lines 2 – 23) involving the first parameter (e.g., parameter of the received frame, col., 11, lines 58 – 67 etc., col., 5, lines 36 – 51).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Ogawa with the teachings of Wilford in order to facilitate usage of a plurality of peripherals means because the peripherals would enhance the handling the information associated with the pointer, and the parameter information would help the software to process information for the circuit.

As per claim 19, Ogawa and Wilford teach the claimed limitation as rejected under claims 16-18. Wilford also teaches a first plurality (e.g., use of modules of memory and/or memory controller that are internal and not external, figures 9, 10, 15, 26, col., 48, lines 39 - 58) of said peripheral means (e.g., use of modules of memory and/or memory controller, figures 9, 10, 15, 26) that are internal (e.g., use of modules of memory and/or memory controller that are internal and not external, figures 9, 10, 15, 26, col., 48, lines 39 - 58) and a second plurality (e.g., use of modules of memory and/or memory controller that are external and not internal, figures 9, 10, 15, 26, col., 48, lines 25 - 37) of said peripheral means (e.g., use of modules of memory

and/or memory controller, figures 9, 10, 15, 26) that are external (e.g., use of modules of memory and/or memory controller that are external and not internal, figures 9, 10, 15, 26, col., 48, lines 25 - 37).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Ogawa with the teachings of Wilford in order to facilitate internal and external peripheral means. The internal peripherals would enhance supporting information that is within the processing means, while the external peripherals would enhance supporting information that is outside the processing means.

As per claim 20, Ogawa and Wilford teach the claimed limitation as rejected under claims 16-19. Wilford also teaches means for interfacing to said first network (e.g., col., 4, lines 46 – 65) configured to de-frame (e.g., col., 2, lines 55 – 67) in compliance with a plurality of network protocol (e.g., col., 4, lines 46 – 65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Ogawa with the teachings of Wilford in order to facilitate interfacing to a network, to de-frame and support a plurality of network protocol because the de-framing would enhance handling of the information over the network according to the network protocol used. The network would support sending information from one device to another device. The network protocols would provide rules for transferring information among the devices.

Note: The Examiner has cited particular columns and line numbers and/or paragraphs and/or sections and/or page numbers in the reference(s) as applied to the claims above for the convenience of the Appellant. Although the specified citations are representative of the teachings of the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the Appellant in preparing responses, to fully consider the references in entirety, as potentially teaching, all or part of the claimed invention, as well as the context of the passage, as taught by the prior art or disclosed by the Examiner.

(11) Response to Arguments

First Ground of Rejection (1) (pages 6 to 10 of the appeal brief)

Claims 1, 8, 10 and 12 (Note: pages 6 to 10 of the appeal brief that represent first ground of rejection (1) for claims 1, 8, 10 and 12 **do not contain any arguments** regarding claimed **limitations of the dependent claims 8, 10 and 12)**

Appellant's arguments (regarding claim 1):

(1), "Ogawa 5,936,966 does not disclose or suggest **reading a pointer for a first parameter within an incoming packet** as presently claimed"

(2) Ogawa does not disclose or suggest the claimed first parameter within an incoming packet **from a first network**"

(3) "**Appendix A, pages A-4 and A-5** of the appeal brief shows that pointer in the TCP protocol is part of the fourth transport layer of the OSI mode and the transport layer and the data link layer are not even adjoining layers in the OSI model"

(4) "Contrary to the **assertion by the Examiner** the TCP object pointer appears to have no connection to the MAC header data of Ogawa"

(5) "Ogawa does not explicitly or inherently disclose a step for **reading a pointer for a first parameter within an incoming packet** as presently claimed"

(6) "Ogawa does not explicitly or inherently disclose **processing the first parameter in accordance with the pointer to produce a second parameter**"

(7) "The **Examiner asserts** Ogawa discusses processing the unidentified MAC header data element in accordance with the TCP object pointer"

(8) "**Nothing in the Ogawa** talk about processing any of the elements in the MAC header data in accordance with the TCP object pointer"

(9) "Contrary to the Examiner's assertion, Ogawa appears to be **silent** regarding a step for **processing a first parameter in accordance with a pointer to produce a second parameter** as presently claimed"

(10) "**None of the elements of Ogawa** appear to be the product of some unidentified processing of an unidentified MAC header data element in accordance with the TCP object pointer, Therefore, Ogawa does not explicitly or inherently disclose a step for processing a first parameter in accordance with a pointer to produce a second parameter as presently claimed"

(11) "Ogawa does not **explicitly or inherently** disclose **presenting an outgoing packet containing the second parameter for a second network**"

(12) "The **Examiner asserts** that presenting an outgoing packet on a second network containing the unidentified element"

(13) "**Nothing in any other section of Ogawa** appears to mention the retrieval key data signal SDK2 being part of an outgoing packet on some unidentified second network, Therefore, Ogawa does not explicitly or inherently disclose a step for presenting an outgoing packet containing a second parameter for a second network as presently claimed"

(14) "In **summary**, Ogawa does not explicitly or inherently disclose (A) reading a pointer for a first parameter within an incoming packet, (B) processing the first parameter in accordance with the pointer to produce a second parameter and (C) presenting an outgoing packet containing the second parameter for a second network. The rejections appear to be a series of unrelated paragraphs that do not arrange the elements as claimed as required by Verdegaal Bros. As such, anticipation has not been established and the rejection should be reversed".

Examiner's response:

The Examiner respectfully disagrees in response to Appellant's arguments. (Note: the **Appellant** has made fourteen arguments for only three steps of the claim 1, which contain broadly claimed subject matter. **In fact,** the claimed subject matter of the claimed invention is **so broad** that several portions and several elements of the Ogawa are pertinent to and read upon the claimed subject matter of the claim 1. With fourteen arguments and the Appellant's assertions, the Appellant demonstrates that the Ogawa neither disclose a single step nor a single element of each of the steps of the claimed subject matter of the claim 1, which the Examiner based on the below presented evidence as taught by the reference strongly acknowledges is not true).

The Examiner would like to reveal Ogawa's teachings as follows **in response to the Appellant's arguments**:

Ogawa's teachings and disclosure demonstrate a method (e.g., col., 3, lines 44 – 59) bridging (e.g., usage of bridge, col., 5, lines 11 – 15, also usage of bridging between two networks, usage of gateway, **router** (similar to the brief summary of invention mentioning usage of router by the application under prosecution), also inherent limitations of WAN, col., 1, line 61 – col., 2, line 29) an incoming packet (e.g., col., 4, line 65 – col., 5, line 6, also figure 6, col., 2, lines, usage of frame data, col., 1, lines 21 – 22, packet type of packet, figure 23, also inherent limitations of packet switching networks and packet switching system, transport packet, col., 15, lines 63 – 67, inherent usage of packet of TCP and IP protocols for frame data, col., 13, lines 23 – 54,) from a first network to a second network (e.g., col., 5, lines 11 – 15, e.g., use of internetwork repeater between first and second networks for handling packets, col., 12, lines 41 – 49, col., 2, lines 5 – 14, also usage of bridging between two networks, usage of bridge, gateway, **router** (similar to the brief summary of invention mentioning usage of router by the application under prosecution), also inherent limitations of WAN, col., 1, line 61 – col., 2, line 29),

Response to the arguments 1 and 5: **reading a pointer** (e.g., offset/flag, length, col., 13, lines 50 –55, signal and/or flag, reading an offset having inherent index / position, figure 21, packet type, figure 23, frame data with synchronization signal, selection signal, length, col., 3, lines 48 – 59, incoming packet containing header information signaling which protocol i.e., IP or IPX etc., col., 13, lines 42 - 54) is used for the supplied parameters, col., 13, lines 12 – 21, col., 15, lines 54 - 66), **for a first parameter** (e.g., parameter of the received frame, col., 11, lines 58 – 67, col., 13, lines 15 – 21, header parameter, protocol information, length information, destination network address, frame length, destination port number, source network address, source port number, col., 8, lines 1 – 18, packet type, figure 23, header length, protocol

information, col., 13, lines 24 – 29, parameter having a data length of certain number of bits, destination and source socket numbers, col., 18, lines 19 - 42) **within an incoming** (e.g., usage of queue / memory for input port, figure 27) **packet** (e.g., col., 12, lines 53 – 63, figure 5, col., 4, line 65 – col., 5, line 6, also col., 2, lines, usage of frame data, col., 1, lines 21 – 22, also inherent limitations of packet switching networks and packet switching system, transport packet, col., 15, lines 63 – 67, inherent usage of packet of TCP and IP protocols for frame data, col., 13, lines 23 – 54, packet type of packet, figure 23, usage of queue / memory for input port, figure 27)

Response to the argument 2: **from a first network** (e.g., col., 5, lines 11 – 15, use of internetwork repeater between first and second networks, col., 12, lines 41 – 49, col., 2, lines 5 – 14, also usage of bridging between two networks, usage of bridge, gateway, **router** (similar to the brief summary of invention mentioning usage of router by the application under prosecution), also inherent limitations of WAN, col., 1, line 61 – col., 2, line 29),

Response to the arguments 6 and 9: **processing said first parameter** (e.g., parameter of the received frame, col., 11, lines 58 – 67, col., 13, lines 15 – 21, header parameter, protocol information, length information, destination network address, frame length, destination port number, source network address, source port number, col., 8, lines 1 – 18, packet type, figure 23, header length, protocol information, col., 13, lines 24 – 29, parameter having a data length of certain number of bits, destination and source socket numbers, col., 18, lines 19 - 42) **in accordance with said pointer** (e.g., offset/flag, col., 13, lines 50 –55, signal/flag reading an offset having inherent index / position, figure 21, packet type, figure 23) **to produce a second parameter** (e.g., PID / MAC address based on table entries and received data frame, col., 9, lines 7 – 24, LLC/SNAP or the LAN emulation header added to create a CPCS-PDU pay-load

portion of the AAL-5 layer, col., 19, lines 23 – 30, addition of linked information as per target, col., 20, lines 4 – 18, usage of CAM – contents addressable memory and executing table retrieval based on protocol and selectively fetching output information, col., 4, lines 52 - 67),

Response to the argument 11: **presenting an outgoing** (e.g., adding information to the packet being built for outgoing, col., 4, lines 3 – 12, col., 4, lines 45 – 54, usage of queue / memory for output port, figure 27, also, iterations of building outgoing packet information is shown in figures 24, 25, creation of packet information including pay-load information based on protocol used, col., 19, lines 25 - 29) **packet** (e.g., col., 8, lines 50 – 63) **containing said second parameter** (e.g., col., 9, lines 7 – 24, header parameter, protocol information, length information, destination network address, frame length, destination port number, source network address, source port number, col., 8, lines 1 – 18, packet type, figure 23, header length, protocol information, col., 13, lines 24 – 29, parameter having a data length of certain number of bits, destination and source socket numbers, col., 18, lines 19 - 42) **for a second network** (e.g., col., 5, lines 11 – 15, use of internetwork repeater between first and second networks, col., 12, lines 41 – 49, col., 2, lines 5 – 14, also usage of bridging between two networks, usage of bridge, gateway, router, also inherent limitations of WAN, col., 1, line 61 – col., 2, line 29).

Response to the argument 14: **Hence**, the Examiner acknowledges that Ogawa teaches / discloses **each and every** claimed elements, limitations, steps and the claimed invention as a whole. Besides Ogawa's teachings, **one of ordinary skilled in the art** at the time of the invention **very well knows** what is a bridge, gateway, router, WAN, incoming packet, outgoing packet, offset, length, pointer, etc. and there uses, regarding the claimed invention (that is also taught by the Ogawa as mapped above). The Examiner would like to provide the **meaning and**

uses of the well-known items to one of ordinary skilled in the art. For example, a bridge is used for **literally** bridging. The **bridge** is a device that connects networks using the same communication protocols or **different protocols** so that the information can be passed **from one network to the other network**. The bridge is a device that connects two LANs (local area networks) whether or not they use the same protocols and allows information **to flow between** them. The bridge router is a device that supports the functions of both a bridge and router and links two segments of a local or wide are network **passing packets of data** between the segments as necessary and **uses addresses** for routing. A **router** is an intermediary device on a communications network that expedites **message delivery**. A router receives **transmitted messages** and forwards them to their correct destinations over the available route. On an interconnected set of local area networks including those based on **differing architectures and protocols** a router serves the somewhat different function of acting as a link between LANs and **enabling messages** to be sent from one to another. Routing is a process of forwarding **packets between networks from source to destination**. A **packet** is a unit of information **transmitted as a whole** (hence inherent **contains parameters**) from one device to another on a network. In packet switching networks a trasmission unit of fix maxium size that consists of binary digits **respresenting** (hence equivalent of the pointer of having values 1, 4, 3 etc of figure 5 of the specification of this application under examination) both **data and a header** containing **an identification number**, source and destination **addresses** and sometimes error **control** data (hence equivalent of the pointer of having values 1, 4, 3 etc of figure 5 of the specification of this application under examination). A **gateway** is a device that connects networks using different communication protocols so that information can be passed from one network to the other

network. A gateway both transfers information **and converts** it to a form compatible with **the protocols** used by the receiving network. **Offset** is a number in **relative addressing** methods that tells **how far from** a starting point a particular item is located. **Pointer** is a **variable** that contains the **location (address)** of some data rather than the data itself. An **address** is a **number** specifying a location where data is stored or **a name** or **token specifying** a particular component related to the network **or** to **reference** a particular storage location. **Length** is a number of units of storage space occupied by an item and **typically** measured in **bits, bytes or blocks**. **Frame** is a unit of transmission that contains the start bit that precedes a character and contain a **flag, address, control, data**, frame **check sequence**, etc. **Frames** are identifiable through start and/or boundary markers. The start and/or boundary markers are used for **delineating** frame packets to **distinguish data frame packets** from other data traffic carried by the network. **Encoding / Encryption** is a process of encoding data to prevent unauthorized access during transmission, usually based on one or more **keys or codes** that are essential for encoding/**decoding** or returing the data to **readable form**.

Further, **the specification of this application under examination**, page 5, lines 19 – 21, also clearly states; the system (bridging between to networks) is any assembly including multiplexer or any other assembly; page 5, lines 19 – 21, clearly states; **the protocols** supported are IP, IPX **or the like**; page 12, lines 18 – 21, clearly states; **a signal can be offset or length or pointer, etc**. The specification of this application **itself contradicts** by providing multiple pointer definitions, **for example, figure 4, block 154 clearly mentions** that **pointer is read processing type pass parameters to peripherals**; **the pointer being just a data type representing one of a numerical value in a packet**, please see figure 5. The claimed

limitations of **claim 4** i.e., "at least one of the **peripheral blocks identified by the pointer** prior to processing" **again contradicts** with the other portions of the specification. Also, page 22, lines 16 –20 of the specification, clearly states, "While the invention has been particularly shown and described with reference to the preferred embodiments thereof, will be understood by those skilled in the art that various changes form and details may be made without departing from the spirit and **scope** of the invention". The Appellant has used "pointer", "offset", etc., with several different meanings through out the specification and the claims. Since, Appellant's claims contain broadly claimed subject matter, it clearly reads upon the Examiner's interpretation of the claimed subject matter.

Response to the argument 3: **Appellant's assertions**, "Appendix A, pages A-4 and A-5 of the appeal brief shows that pointer in the TCP protocol is part of the fourth transport layer of the OSI model and the transport layer and the data link layer are not even adjoining layers in the OSI model", **is misleading** because the **claimed limitations** of the claim 1 **are not limited to** any of the **particular protocol** (TCP or any other protocol etc), **particular** fourth transport **layer of the OSI model**, the data link layer, **adjoining layers in the OSI model** etc. Also, the claimed limitations i.e., **incoming packet, outgoing packet, pointer, first parameter, second parameter** etc, are **not limited to a particular layer of the OSI model** (please see the claim), which the Appellant is very much concerned.

In fact, the Appellant's provided Appendix A, pages A- 3 to5 (dated 1998) of the appeal brief clearly **also** supports (**provide more evidence**), that **internetworking** supports usage of **bits, frames, packets across different networks,** communication **at different layers**, i.e., physical layer, data link layer, network layer, transport layer etc. The data link layer description

further goes into explanation of not only **receiving** as asserted by the Appellant, but also **transmitting / sending** using **Ethernet, MAC** etc. The **different protocols and packets** are also clearly explained. The Ogawa clearly states, "The present invention relates to **network frame data** based on **any arbitrary protocol** of a **plurality of protocol hierarchies** defined from **a physical layer to upper layers** (please see col., 1, lines 14-17).

Response to the argument 4: **Appellant's assertions**, "Contrary to the assertion by the Examiner the TCP object pointer appears to have no connection to the MAC header data of Ogawa", **is misleading** because the prosecution history of this case clearly shows that **no one** including the Examiner has mentioned or **asserted** about the TCP object pointer appears to have a connection to the MAC header data and the **claimed limitations** of the claim 1 **are not limited to** whether or not the TCP object pointer to have a connection to the MAC header data, which the Appellant is very much concerned.

Response to the argument 7: **Appellant's assertions**, "The Examiner asserts Ogawa discusses processing the unidentified MAC header data element in accordance with the TCP object pointer", **is misleading** because the prosecution history of this case clearly shows that **no one** including the Examiner has mentioned or **asserted** about processing the unidentified MAC header data element in accordance with the TCP object pointer and the **claimed limitations** of the claim 1 **are not limited to** whether or not the processing the unidentified MAC header data element is in accordance with the TCP object pointer, which the Appellant is very much concerned.

Response to the argument 8: **Appellant's assertions**, "Nothing in the Ogawa talk about processing any of the elements in the MAC header data in accordance with the TCP object

pointer", **is misleading** because the prosecution history of this case clearly shows that **no one** including the Examiner has mentioned or **asserted** about processing any of the elements in the MAC header data in accordance with the TCP object pointer, which is **not relevant** with the claimed invention and the **claimed limitations** of the claim 1 **are not limited to** whether or not the processing any of the elements in the MAC header data is in accordance with the TCP object pointer, which the Appellant is very much concerned.

Response to the argument 10: **Appellant's assertions**, "None of the elements of Ogawa appear to be the product of some unidentified processing of an unidentified MAC header data element in accordance with the TCP object pointer", **is misleading** because the prosecution history of this case clearly shows that **no one** including the Examiner has mentioned or **asserted** about the elements of Ogawa appear to be the product of some unidentified processing of an unidentified MAC header data element in accordance with the TCP object pointer, which is **not relevant** with the claimed invention and the **claimed limitations** of the claim 1 **are not limited to** whether or not the elements of appear to be the product of some unidentified processing of an unidentified MAC header data element in accordance with the TCP object pointer, which the Appellant is very much concerned.

Response to the argument 12: **Appellant's assertions**, "The Examiner asserts that presenting an outgoing packet on a second network containing the unidentified element", **is misleading** because the prosecution history of this case clearly shows that **no one** including the Examiner has mentioned or **asserted** about presenting an outgoing packet on a second network **containing the unidentified element**, which is **not relevant** with the claimed invention and the **claimed limitations** of the claim 1 **are not limited to** whether or not presenting an outgoing

packet on a second network containing the unidentified element, which the Appellant is very much concerned.

Response to the argument 13: **Appellant's assertions**, "Nothing in any other section of Ogawa appears to mention the retrieval key data signal SDK2 being part of an outgoing packet on some unidentified second network", **is misleading** because the prosecution history of this case clearly shows that **no one** including the Examiner has mentioned or **asserted** about the retrieval key data signal SDK2 being part of an outgoing packet on some unidentified second network, which is **not relevant** with the claimed invention and the **claimed limitations** of the claim 1 **are not limited to** whether or not the retrieval key data signal SDK2 being part of an outgoing packet on some unidentified second network, which the Appellant is very much concerned.

Response to the argument 14: **In fact,** regarding the limitations of the claim 1, **a value of a pointer** (1, 4, 3 etc of figure 5 of the specification of this application under examination) is read and processing of the first parameter is done in accordance with **the value of the pointer** (see figure 5 of the specification of this application under examination for clarification). The specification of this application under examination itself **contradicts** by providing multiple pointer definitions, **for example,** figure 4, block 154 clearly mentions that pointer is read processing type pass parameters to peripherals; the pointer being just a data type representing one of a numerical value in a packet, please see figure 5. In fact, a broadest interpretation by one of ordinary skilled in the art for a **pointer** is anything **that indicates something**, and/or **a variable that holds the address or reference of a location**.

Further, **contrary to Appellant's assertions**, limitations, "outgoing packet" **is not limited** to a packet outgoing from the circuit or database etc, as the claimed invention does not specify outgoing in reference to anything. Limitations, "present an outgoing packet" **is not limited to** generating or producing, etc., of an outgoing packet. Also, the specification of this application under examination does not specifically mention that the second parameter is limited to a particular type of parameter, and to not consider, offset of the packet and/or pointer of the packet and/or length of the packet and/or other data of the packet that are outgoing something, as the second parameter. The claimed invention does not specifically mention that the second network and/or first network is limited to a particular type of network etc. Further, limitations, "first parameter" is not limited to a particular type of parameter or a different type of a parameter, and to not consider, offset of the packet and/or pointer of the packet and/or length of the packet and/or other data of the packet that are outgoing something, as the second parameter etc., Also, the specification of this application under examination clearly states, page 12, lines 18 – 21, a signal can be offset or length, etc. Further, **contrary to Appellant's assertions** limitations, "reading a pointer" of the claim 1 is **not limited to the pointer being part of the incoming packet**. Further, the claimed invention of claim 1 not **limited to** usage of an **Ethernet frame, MAC destination, MAC source, PDI, reading the first parameter off the incoming packet, Once the parameter is found ..., reading implemented by a parser circuit, matching address (contrary** to producing parameter of the claim 1**), processing implemented by a number of peripherals, assembling the parameter, framing an outgoing frame, then transmitting the outgoing frame**, and/or presenting implemented **by an assembler circuit,** which the Appellant is very much concerned.

Thus, a method of bridging an incoming packet from a first network to a second network comprising the steps of reading a pointer **for** a first parameter within the incoming packet, processing the first parameter in accordance with the pointer to produce a second parameter and presenting an outgoing packet containing the second parameter **for** the second network is clearly understood and based on the presented evidence as taught by the reference and interpreted by the Examiner, these limitations as claimed are indeed not novel and hence the rejection should be maintained.

First Ground of Rejection (2) (page 11 line 1 to page 15 line 6 of the appeal brief)

Claim 16

Appellant's arguments (regarding claim 16):

(1), "Ogawa does not disclose or suggest a means for **reading a pointer for a first parameter within an incoming packet from a first network** as presently claimed"

(2) **Ogawa appears to be silent** regarding a **circuit structure** within the data receiving device"

(3) "MAC layer is part of the second data link layer of the OSI model and the object pointer in the TCP protocol is part of the fourth transport layer of the OSI mode see **Appendix A, pages A-4 and A-5** of the appeal brief shows that pointer in the TCP protocol is part of the fourth transport layer of the OSI mode and the transport layer and the data link layer are not even adjoining layers in the OSI model"

(4) "Contrary to the **assertion by the Examiner** the TCP object pointer appears to have no connection to the MAC header data of Ogawa"

(5) "Ogawa does not explicitly or inherently disclose a means for **reading a pointer for a first parameter within an incoming packet** as presently claimed"

(6) "Ogawa does not explicitly or inherently disclose a means for **processing the first parameter in accordance with the pointer to produce a second parameter**"

(7) "The **Examiner asserts** Ogawa discusses processing the unidentified MAC header data element in accordance with the TCP object pointer"

(8) "**Nothing in the Ogawa** talk about processing any of the elements in the MAC header data in accordance with the TCP object pointer"

(9) "Contrary to the Examiner's assertion, Ogawa appears to be **silent** regarding a step for **processing a first parameter in accordance with a pointer to produce a second parameter** as presently claimed"

(10) "**None of the elements of Ogawa** appear to be the product of some unidentified processing of an unidentified MAC header data element in accordance with the TCP object pointer, Therefore, Ogawa does not explicitly or inherently disclose a step for processing a first parameter in accordance with a pointer to produce a second parameter as presently claimed"

(11) "Ogawa does not **explicitly or inherently** disclose a means for **presenting an outgoing packet containing the second parameter for a second network**"

(12) "The **Examiner asserts** that presenting an outgoing packet on a second network containing the unidentified element"

(13) "**Nothing in any other section of Ogawa** appears to mention the retrieval key data signal SDK2 being part of an outgoing packet on some unidentified second network, Therefore,

Ogawa does not explicitly or inherently disclose a step for presenting an outgoing packet containing a second parameter for a second network as presently claimed"

(14) "In **summary**, Ogawa does not explicitly or inherently disclose a circuit comprising (A) means for reading a pointer for a first parameter within an incoming packet, (B) means for processing the first parameter in accordance with the pointer to produce a second parameter and (C) means for presenting an outgoing packet containing the second parameter. The rejections appear to be a series of unrelated paragraphs that do not arrange the elements as claimed as required by Verdegaal Bros. As such, anticipation has not been established and the rejection should be reversed".

Examiner's response:

The Examiner respectfully disagrees in response to Appellant's arguments. (Note: the Appellant has made fourteen arguments for only three means of the claim 16, which contain broadly claimed subject matter. **In fact,** the claimed subject matter of the claimed invention is **so broad** that **several portions** and **several elements** of the Ogawa are pertinent to and read upon the claimed subject matter of the claim 16. With fourteen arguments and the Appellant's assertions, the Appellant demonstrates that the Ogawa neither disclose a single means nor a single element of each of the means of the claimed subject matter of the claim 16, which the Examiner based on the below presented evidence as taught by the reference strongly acknowledges is not true).

The Examiner would like to reveal Ogawa's teachings as follows **in response to the Appellant's arguments**:

Ogawa's teachings and disclosure demonstrate a circuit (e.g., one of the circuits of abstract, one of the circuits of figure 1, col., 3, lines 44 – 59, usage of bridge (hence inherent circuit), col., 5, lines 11 – 15, also usage of bridging between two networks, usage of gateway, router, also use of WAN that contain circuits to do processing etc, col., 1, line 61 – col., 2, line 29),

Response to the arguments 1 and 5: **means for** (e.g., one of the circuits of abstract, one of the circuits of figure 1, col., 3, lines 44 – 59, usage of bridge hence inherent use of circuit, col., 5, lines 11 – 15, also usage of bridging between two networks, usage of gateway, **router** and the router components that is similar to the application under prosecution that contains the brief summary of invention and the specification mentioning usage of router and components, also use of WAN that contain circuits to do processing etc, col., 1, line 61 – col., 2, line 29) **reading a pointer** (e.g., offset/flag, length, col., 13, lines 50 –55, signal and/or flag, reading an offset having inherent index / position, figure 21, packet type, figure 23, frame data with synchronization signal, selection signal, length, col., 3, lines 48 – 59, incoming packet containing header information signaling which protocol i.e., IP or IPX etc., col., 13, lines 42 - 54) is used for the supplied parameters, col., 13, lines 12 – 21, col., 15, lines 54 - 66), **for a first parameter** (e.g., parameter of the received frame, col., 11, lines 58 – 67, col., 13, lines 15 – 21, header parameter, protocol information, length information, destination network address, frame length, destination port number, source network address, source port number, col., 8, lines 1 – 18, packet type, figure 23, header length, protocol information, col., 13, lines 24 – 29, parameter having a data length of certain number of bits, destination and source socket numbers, col., 18, lines 19 - 42) **within an incoming** (e.g., usage of queue / memory for input port, figure 27) **packet** (e.g.,

col., 12, lines 53 – 63, figure 5, col., 4, line 65 – col., 5, line 6, also col., 2, lines, usage of frame data, col., 1, lines 21 – 22, also inherent limitations of packet switching networks and packet switching system, transport packet, col., 15, lines 63 – 67, inherent usage of packet of TCP and IP protocols for frame data, col., 13, lines 23 – 54, packet type of packet, figure 23, usage of queue / memory for input port, figure 27) **complaint with a network protocol** (e.g., col., 12, lines 53 – 63, figure 5, col., 4, line 65 – col., 5, line 6, also col., 2, lines, usage of frame data based on a network protocol, col., 1, lines 21 – 22, also inherent limitations of packet switching networks and packet switching system, transport packet, col., 15, lines 63 – 67, inherent usage of packet of TCP and IP protocols for frame data, col., 13, lines 23 – 54, packet type of packet that is protocol specific, figure 23, usage of queue / memory for input port, figure 27)

from a first network (e.g., col., 5, lines 11 – 15, use of internetwork repeater between first and second networks, col., 12, lines 41 – 49, col., 2, lines 5 – 14, also usage of bridging between two networks, usage of bridge, gateway, router, also inherent limitations of WAN, col., 1, line 61 – col., 2, line 29), In response to Appellant's argument that the references fail to show certain features of Appellant's invention, it is noted that the features upon which Appellant relies, "**from a first network**", are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). The First inquiry must be into exactly what the claims define. See *In re Wilder*, 166 USPQ 545, 548 (CCPA 1970).

In fact, **the specification of this application under examination**, page 5, lines 19 – 21, contain **several** components that can be used for the implementation of the "**means for**" limitations, please see, page 5, lines 19 – 21, page 22, lines 16 –20 of the specification.

Note: The **Appellant's assertions** that the claimed invention has **a circuit (single) comprising three circuit means** for reading, processing and presenting (please see claim 16) **contradicts** with the another **Appellant's assertions** that the figure 2 which is part of the specification of the application under prosecution discloses **an assembly (102)** (not a single circuit as claimed) comprising three circuit means for reading, processing and presenting. **In fact**, the claimed invention **does not provide support** on how the three circuit means for reading, processing and presenting are **different from each other** and **why and what is that** the same circuit cannot implement limitations of other means. The claimed invention also **do not support on how** the claimed **circuits are different** than the well known circuits including the circuits cited by the references.

Response to the argument 2: In response to Appellant's argument that the references fail to show certain features of Appellant's invention, it is noted that the features upon which Appellant relies, "a **circuit structure** within the data receiving device", are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). The First inquiry must be into exactly what the claims define. See *In re Wilder*, 166 USPQ 545, 548 (CCPA 1970), What is claimed is, **a circuit** (e.g., Ogawa discloses usage of one of the circuits of abstract, one of the circuits of figure 1, col., 3, lines 44 –

59, usage of bridge, col., 5, lines 11 – 15, also usage of bridging between two networks, usage of gateway, router, also use of WAN that contain circuits to do processing etc, col., 1, line 61 – col., 2, line 29), **means for** reading / processing / presenting (e.g., circuits of abstract, circuits of figure 1, col., 3, lines 44 – 59, usage of bridge, col., 5, lines 11 – 15, also usage of bridging between two networks, usage of gateway, router, the router components that is similar to the application under prosecution that contains the brief summary of invention and the specification mentioning usage of router and components, also use of WAN that contain circuits to do processing etc, col., 1, line 61 – col., 2, line 29),

Response to the arguments 6 and 9: **means for** (e.g., circuits of abstract, circuits of figure 1, col., 3, lines 44 – 59, usage of bridge, col., 5, lines 11 – 15, also usage of bridging between two networks, usage of gateway, router, the router components that is similar to the application under prosecution that contains the brief summary of invention and the specification mentioning usage of router and components, also use of WAN that contain circuits to do processing etc, col., 1, line 61 – col., 2, line 29) **processing said first parameter** (e.g., parameter of the received frame, col., 11, lines 58 – 67, col., 13, lines 15 – 21, header parameter, protocol information, length information, destination network address, frame length, destination port number, source network address, source port number, col., 8, lines 1 – 18, packet type, figure 23, header length, protocol information, col., 13, lines 24 – 29, parameter having a data length of certain number of bits, destination and source socket numbers, col., 18, lines 19 - 42) **in accordance with said pointer** (e.g., offset/flag, col., 13, lines 50 –55, signal/flag reading an offset having inherent index / position, figure 21, packet type, figure 23) **to produce a second parameter** (e.g., PID / MAC address based on table entries and received data frame, col., 9, lines 7 – 24, LLC/SNAP or

the LAN emulation header added to create a CPCS-PDU pay-load portion of the AAL-5 layer, col., 19, lines 23 – 30, addition of linked information as per target, col., 20, lines 4 – 18, usage of CAM – contents addressable memory and executing table retrieval based on protocol and selectively fetching output information, col., 4, lines 52 - 67),

Response to the argument 11: **means for** (e.g., circuits of abstract, circuits of figure 1, col., 3, lines 44 – 59, usage of bridge, col., 5, lines 11 – 15, also usage of bridging between two networks, usage of gateway, router, the router components that is similar to the application under prosecution that contains the brief summary of invention and the specification mentioning usage of router and components, also use of WAN that contain circuits to do processing etc, col., 1, line 61 – col., 2, line 29) **presenting an outgoing** (e.g., usage of queue / memory for output port, figure 27, also, iterations of building outgoing packet information is shown in figures 24, 25, creation of packet information including pay-load information based on protocol used, col., 19, lines 25 - 29) packet (e.g., col., 8, lines 50 – 63) **containing said second parameter** (e.g., col., 9, lines 7 – 24, header parameter, protocol information, length information, destination network address, frame length, destination port number, source network address, source port number, col., 8, lines 1 – 18, packet type, figure 23, header length, protocol information, col., 13, lines 24 – 29, parameter having a data length of certain number of bits, destination and source socket numbers, col., 18, lines 19 - 42)

for a second network (e.g., col., 5, lines 11 – 15, use of internetwork repeater between first and second networks, col., 12, lines 41 – 49, col., 2, lines 5 – 14, also usage of bridging between two networks, usage of bridge, gateway, router, also inherent limitations of WAN, col., 1, line 61 – col., 2, line 29), also, In response to Appellant's argument that the references fail to

show certain features of Appellant's invention, it is noted that the features upon which Appellant relies, "**for a second network**", are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). The First inquiry must be into exactly what the claims define. See *In re Wilder*, 166 USPQ 545, 548 (CCPA 1970),

Response to the argument 14: **Hence**, the Examiner acknowledges that Ogawa teaches / discloses **each and every** claimed elements, limitations, steps and the claimed invention as a whole. Besides Ogawa's teachings, **one of ordinary skilled in the art** at the time of the invention **very well knows** what is a bridge, gateway, router, WAN, incoming packet, outgoing packet, offset, length, pointer, etc., and there uses regarding the claimed invention (that is also taught by the Ogawa as mapped above). The Examiner would like to **again** provide the **meaning and uses of the well-known items** to one of ordinary skilled in the art (that is related to the claimed subject matter of claim). For example, a bridge is used for **literally** bridging. The **bridge** is a device that connects networks using the same communication protocols or **different protocols** so that the information can be passed **from one network to the other network**. The bridge is a device that connects two LANs (local area networks) whether or not they use the same protocols and allows information **to flow between** them. The bridge router is a device that supports the functions of both a bridge and router and links two segments of a local or wide are network **passing packets of data** between the segments as necessary and **uses addresses** for routing. A **router** is an intermediary device on a communications network that expedites **message delivery**. A router receives **transmitted messages** and forwards them to their correct

destinations over the available route. On an interconnected set of local area networks including those based on **differing architectures and protocols** a router serves the somewhat different function of acting as a link between LANs and **enabling messages** to be sent from one to another. Routing is a process of forwarding **packets between networks from source to destination**. A **packet** is a unit of information **transmitted as a whole** (hence inherent **contains parameters**) from one device to another on a network. In packet switching networks a trasmission unit of fix maxium size that consists of binary digits **respresenting** (hence equivalent of the pointer of having values 1, 4, 3 etc of figure 5 of the specification of this application under examination) both **data and a header** containing **an identification number**, source and destination **addresses** and sometimes error **control** data (hence equivalent of the pointer of having values 1, 4, 3 etc of figure 5 of the specification of this application under examination). A **gateway** is a device that connects networks using different communication protocols so that information can be passed from one network to the other network. A gateway both transfers information **and converts** it to a form compatible with **the protocols** used by the receiving network. **Offset** is a number in **relative addressing** methods that tells **how far from** a starting point a particular item is located. **Pointer** is a **variable** that contains the **location** (**address**) of some data rather than the data itself. An **address** is a **number** specifying a location where data is stored or **a name** or **token specifying** a particular component related to the network **or** to **reference** a particular storage location. **Length** is a number of units of storage space occupied by an item and **typically** measured in **bits, bytes or blocks. Frame** is a unit of transmission that contains the start bit that precedes a character and contain a **flag, address, control, data**, frame **check sequence**, etc. **Frames** are identifiable through start and/or boundary

markers. The start and/or boundary markers are used for **delineating** frame packets to **distinguish data frame packets** from other data traffic carried by the network. **Encoding / Encryption** is a process of encoding data to prevent unauthorized access during transmission, usually based on one or more **keys or codes** that are essential for encoding/**decoding** or returing the data to **readable form**.

Further, **the specification of this application under examination**, page 5, lines 19 – 21, also clearly states; the system (bridging between to networks) is any assembly including multiplexer or any other assembly; page 5, lines 19 – 21, clearly states; **the protocols** supported are IP, IPX **or the like**; page 12, lines 18 – 21, clearly states; **a signal can be offset or length or pointer, etc**. The specification of this application **itself contradicts** by providing multiple pointer definitions, **for example, figure 4, block 154 clearly mentions** that **pointer is read processing type pass parameters to peripherals**; **the pointer being just a data type representing one of a numerical value in a packet**, please see figure 5. The claimed limitations of **claim 4** i.e., "at least one of the **peripheral blocks identified by the pointer** prior to processing" **again contradicts** with the other portions of the specification. Also, specification of this application **does not** specifically **mention** that the **circuit is limited to a particular type of circuit**, **and to not consider**, Network Interface 1 and/or Network Interface 2 and/or External Peripherals and/or Parser circuit and/or Assembler etc other circuits of the application being the claimed circuit.

Also, page 22, lines 16 –20 of the specification, clearly states, "While the invention has been particularly shown and described with reference to the preferred embodiments thereof, will be understood by those skilled in the art that various changes form and details may be made

without departing from the spirit and **scope** of the invention". The Appellant has used "pointer", "offset", etc., with several different meanings through out the specification and the claims. Since, Appellant's claims contain broadly claimed subject matter, it clearly reads upon the Examiner's interpretation of the claimed subject matter.

Response to the argument 3: **Appellant's assertions**, "MAC layer is part of the second data link layer of the OSI model and the object pointer in the TCP protocol is part of the fourth transport layer of the OSI mode see Appendix A, pages A-4 and A-5 of the appeal brief shows that pointer in the TCP protocol is part of the fourth transport layer of the OSI mode and the transport layer and the data link layer are not even adjoining layers in the OSI model", **is misleading** because the **claimed limitations** of the claim 1 **are not limited to** any of the **particular protocol** (TCP or any other protocol etc), MAC layer is part of the second data link layer of the OSI model and the object pointer in the TCP protocol is part of the fourth transport layer of the OSI model, the data link layer, **adjoining layers in the OSI model** etc. Also, the claimed limitations i.e., **incoming packet, outgoing packet, pointer, first parameter, second parameter** etc, are **not limited to a particular layer of the OSI model** (please see the claim), which the Appellant is very much concerned.

In fact, the Appellant's provided Appendix A, pages A- 3 to5 (dated 1998) of the appeal brief clearly **also** supports (**provide more evidence**), that **internetworking** supports usage of **bits, frames, packets across different networks,** communication **at different layers**, i.e., physical layer, data link layer, network layer, transport layer etc. The data link layer description **further** goes into explanation of not only **receiving** as asserted by the Appellant, but also **transmitting / sending** using **Ethernet, MAC** etc. The **different protocols and packets** are

also clearly explained. The Ogawa clearly states, "The present invention relates to **network frame data** based on **any arbitrary protocol** of a **plurality of protocol hierarchies** defined from **a physical layer to upper layers** (please see col., 1, lines 14-17).

Response to the argument 4: **Appellant's assertions**, "Contrary to the assertion by the Examiner the TCP object pointer appears to have no connection to the MAC header data of Ogawa", **is misleading** because the prosecution history of this case clearly shows that **no one** including the Examiner has mentioned or **asserted** about the TCP object pointer appears to have a connection to the MAC header data and the **claimed limitations** of the claim 1 **are not limited to** whether or not the TCP object pointer to have a connection to the MAC header data, which the Appellant is very much concerned.

Response to the argument 7: **Appellant's assertions**, "The Examiner asserts Ogawa discusses processing the unidentified MAC header data element in accordance with the TCP object pointer", **is misleading** because the prosecution history of this case clearly shows that **no one** including the Examiner has mentioned or **asserted** about processing the unidentified MAC header data element in accordance with the TCP object pointer and the **claimed limitations** of the claim 1 **are not limited to** whether or not the processing the unidentified MAC header data element is in accordance with the TCP object pointer, which the Appellant is very much concerned.

Response to the argument 8: **Appellant's assertions**, "Nothing in the Ogawa talk about processing any of the elements in the MAC header data in accordance with the TCP object pointer", **is misleading** because the prosecution history of this case clearly shows that **no one** including the Examiner has mentioned or **asserted** about processing any of the elements in the

MAC header data in accordance with the TCP object pointer, which is **not relevant** with the claimed invention and the **claimed limitations** of the claim 1 **are not limited to** whether or not the processing any of the elements in the MAC header data is in accordance with the TCP object pointer, which the Appellant is very much concerned.

Response to the argument 10: **Appellant's assertions**, "None of the elements of Ogawa appear to be the product of some unidentified processing of an unidentified MAC header data element in accordance with the TCP object pointer", **is misleading** because the prosecution history of this case clearly shows that **no one** including the Examiner has mentioned or **asserted** about the elements of Ogawa appear to be the product of some unidentified processing of an unidentified MAC header data element in accordance with the TCP object pointer, which is **not relevant** with the claimed invention and the **claimed limitations** of the claim 1 **are not limited to** whether or not the elements of appear to be the product of some unidentified processing of an unidentified MAC header data element in accordance with the TCP object pointer, which the Appellant is very much concerned.

Response to the argument 12: **Appellant's assertions**, "The Examiner asserts that presenting an outgoing packet on a second network containing the unidentified element", **is misleading** because the prosecution history of this case clearly shows that **no one** including the Examiner has mentioned or **asserted** about presenting an outgoing packet on a second network **containing the unidentified element**, which is **not relevant** with the claimed invention and the **claimed limitations** of the claim 1 **are not limited to** whether or not presenting an outgoing packet on a second network containing the unidentified element, which the Appellant is very much concerned.

Response to the argument 13: **Appellant's assertions**, "Nothing in any other section of Ogawa appears to mention the retrieval key data signal SDK2 being part of an outgoing packet on some unidentified second network", **is misleading** because the prosecution history of this case clearly shows that **no one** including the Examiner has mentioned or **asserted** about the retrieval key data signal SDK2 being part of an outgoing packet on some unidentified second network, which is **not relevant** with the claimed invention and the **claimed limitations** of the claim 1 **are not limited to** whether or not the retrieval key data signal SDK2 being part of an outgoing packet on some unidentified second network, which the Appellant is very much concerned.

Response to the argument 14: **In fact,** regarding the limitations of the claim 1, **a value of a pointer** (1, 4, 3 etc of figure 5 of the specification of this application under examination) is read and processing of the first parameter is done in accordance with **the value of the pointer** (see figure 5 of the specification of this application under examination for clarification). The specification of this application under examination itself **contradicts** by providing multiple pointer definitions, **for example,** figure 4, block 154 clearly mentions that pointer is read processing type pass parameters to peripherals; the pointer being just a data type representing one of a numerical value in a packet, please see figure 5. In fact, a broadest interpretation by one of ordinary skilled in the art for a **pointer** is anything **that indicates something**, and/or **a variable that holds the address or reference of a location**.

Further, **contrary to Appellant's assertions**, limitations, "outgoing packet" **is not limited** to a packet outgoing from the circuit or database etc, as the claimed invention does not specify outgoing in reference to anything. Limitations, "present an outgoing packet" **is not**

limited to generating or producing, etc., of an outgoing packet. Also, the specification of this application under examination **does not** specifically mention that the **second parameter is limited to a particular type of parameter**, and **to not consider**, offset of the packet and/or pointer of the packet and/or length of the packet and/or other data of the packet that are outgoing something, as the second parameter. Further, limitations, "**first parameter**" is **not limited** to a **particular type of parameter or a different type of a parameter**, and **to not consider**, offset of the packet and/or pointer of the packet and/or length of the packet and/or other data of the packet that are outgoing something, as the second parameter etc., Also, the specification of this application under examination clearly states, page 12, lines 18 – 21, a signal can be offset or length, etc. Further, **contrary to Appellant's assertions** limitations, "reading a pointer" of the claim 1 is **not limited to the pointer being part of the incoming packet**. Further, the claimed invention of claim 1 not **limited to** usage of an **Ethernet frame, MAC destination, MAC source, PDI, reading the first parameter off the incoming packet, Once the parameter is found ..., reading implemented by a parser circuit, matching address (contrary** to producing parameter of the claim 1**), processing implemented by a number of peripherals, assembling the parameter, framing an outgoing frame, then transmitting the outgoing frame**, and/or presenting implemented **by an assembler circuit,** which the Appellant is very much concerned.

Thus, a circuit having means for reading a pointer **for** a first parameter within the incoming packet complaint with a network protocol, means for processing the first parameter in accordance with the pointer to produce a second parameter and means for presenting an outgoing packet containing the second parameter is clearly understood and based on the presented

evidence as taught by the reference and interpreted by the Examiner, these limitations as claimed are indeed not novel and hence the rejection should be maintained.

First Ground of Rejection (3) (pages 15, line 7 through page 17, line 3 of the appeal brief)

Claim 2

Appellant's arguments (regarding claim 2):

(1), "Ogawa does not disclose or suggest **reading a length and an offset for the first parameter** as presently claimed"

(2) "Contrary to the **assertion by the Examiner** Ogawa does not appear to discuss a length and an offset for MAC header data element"

(3) "**Ogawa does not appear** to discuss partitioning an incoming packet in accordance with an unidentified offset and an unidentified length to extract an unidentified MAC header data element"

(4) "Ogawa does not explicitly or inherently disclose a step for **partitioning the incoming packet in accordance with the offset and the length to extract the first parameter prior to processing** as presently claimed"

Examiner's response:

The Examiner respectfully disagrees in response to Appellant's arguments.

The Examiner would like to reveal Ogawa's teachings as follows **in response to the Appellant's arguments**:

Response to the argument 1: Ogawa's teachings and disclosure demonstrate **reading a length and an offset** (e.g., offset/flag, length, col., 13, lines 50 –55, e.g., lines 27 - 65, col., 9 reading an offset having inherent index / position, figure 21, packet type, figure 23) **for said first parameter** (e.g., col., 13, lines 15 – 21, header parameter, protocol information, length information, destination network address, frame length, destination port number, source network address, source port number, col., 8, lines 1 – 18, packet type, figure 23, header length, protocol information, col., 13, lines 24 – 29, parameter having a data length of certain number of bits, destination and source socket numbers, col., 18, lines 19 - 42)

Response to the argument 4: **partitioning said incoming packet** (e.g., retrieving information from the frame / packet, col., 7, lines 54 – 62, lines 27 - 65, col., 9) **in accordance with said offset and said length** (e.g., offset/flag, length, col., 13, lines 50 –55, e.g., lines 27 - 65, col., 9 reading an offset having inherent index / position, figure 21, packet type, figure 23) **to extract said first parameter prior to processing** (e.g., 14th time, 17th time etc iterations of processing after parameter information is received, figure 23, also use of packet information that is utilized to process the packet parameters before processing col., 2, lines 28 - 52).

Response to the argument 2: **Appellant's assertions**, "Contrary to the **assertion by the Examiner** Ogawa does not appear to discuss a length and an offset for MAC header data element", **is misleading** because the prosecution history of this case clearly shows that **no one** including the Examiner has mentioned or **asserted** about length and an offset for MAC header data element and the **claimed limitations** of the claim 2 **are not limited to** whether or not the length and an offset exist **for MAC header data element,** which the Appellant is very much concerned.

Response to the argument 3: **Appellant's assertions**, "partitioning an incoming packet in accordance with an unidentified offset and an unidentified length to extract an unidentified MAC header data element", **is misleading** because the prosecution history of this case clearly shows that **no one** including the Examiner has mentioned or **asserted** about partitioning an incoming packet in accordance with an unidentified offset and an unidentified length **to extract an unidentified MAC header data element**, which is **not relevant** with the claimed invention and the **claimed limitations** of the claim 2 **are not limited to** whether or not the partitioning an incoming packet is in accordance with an unidentified offset and an unidentified length to extract an unidentified MAC header data element, which the Appellant is very much concerned.

Further, **contrary to Appellant's assertions**, limitations, "reading a length and an offset" **is not limited** to **reading** the length and the offset **from the incoming packet**. Limitations, "prior to processing" **is not limited to** prior to processing the first parameter, which the Appellant is very much concerned.

Thus, reading a length and an offset **for** said first parameter and partitioning the incoming packet in accordance with the offset and the length to extract the first parameter prior to processing is clearly understood and based on the presented evidence as taught by the reference and interpreted by the Examiner, these limitations as claimed are indeed not novel and hence the rejection should be maintained.

First Ground of Rejection (4) (pages 17, line 4 through page 18 of the appeal brief)

Claim 17

Appellant's arguments (regarding claim 17):

(1) "**Ogawa does not appear** to discuss partitioning an incoming packet in accordance with an unidentified offset and an unidentified length to extract an unidentified MAC header data element"

(2) "Ogawa does not explicitly or inherently disclose means for **partitioning the incoming packet** as presently claimed"

Examiner's response:

The Examiner respectfully disagrees in response to Appellant's arguments.

The Examiner would like to reveal Ogawa's teachings as follows **in response to the Appellant's arguments**:

Response to the argument 2: **means for** (e.g., circuits of abstract, circuits of figure 1, col., 3, lines 44 – 59, usage of bridge, col., 5, lines 11 – 15, also usage of bridging between two networks, usage of gateway, router, the router components that is similar to the application under prosecution that contains the brief summary of invention and the specification mentioning usage of router and components, also use of WAN that contain circuits to do partitioning of the packets etc, col., 1, line 61 – col., 2, line 29) **partitioning said incoming packet** (e.g., retrieving information from the frame / packet, col., 7, lines 54 – 62, lines 27 - 65, col., 9).

Response to the argument 1: **Appellant's assertions**, "Ogawa does not appear partitioning an incoming packet in accordance with an unidentified offset and an unidentified length to extract an unidentified MAC header data element", **is misleading** because the prosecution history of this case clearly shows that **no one** including the Examiner has mentioned or **asserted** about partitioning an incoming packet in accordance with an unidentified offset and an unidentified length **to extract an unidentified MAC header data element**, which is **not**

relevant with the claimed invention and the **claimed limitations** of the claim 17 **are not limited to** whether or not the partitioning an incoming packet is in accordance with an unidentified offset and an unidentified length to extract an unidentified MAC header data element, which the Appellant is very much concerned.

Further, **contrary to Appellant's assertions**, limitations, "prior to processing" **is not limited to** prior to processing the first parameter, which the Appellant is very much concerned.

Thus, means for partitioning the incoming packet is clearly understood and based on the presented evidence as taught by the reference and interpreted by the Examiner, these limitations as claimed are indeed not novel and hence the rejection should be maintained..

First Ground of Rejection (5) (pages 18 through 20 of the appeal brief)

Claims 3

Appellant's arguments (regarding claim 3):

(1), "Ogawa does not disclose or suggest **a step for downloading the offset, the length, and the pointer prior to reading** as presently claimed"

(2) "Ogawa does not disclose or suggest downloading taking place prior to the alleged reading of the of the TCP object pointer for a first pointer"

Examiner's response:

The Examiner respectfully disagrees in response to Appellant's arguments.

The Examiner would like to reveal Ogawa's teachings as follows **in response to the Appellant's arguments**:

Response to the argument 1: Ogawa's teachings and disclosure demonstrate downloading said offset, said length, and said pointer prior to reading (e.g., lines 27 - 65, col., 9).

Further, **contrary to Appellant's assertions**, limitations, "downloading" **is not limited** to **downloading from the first network,** as the claimed invention does not specify **who is** performing **downloading** or **downloading** the offset, the length and the pointer **from the first network** or **downloading the offset,** the length and the pointer **from the incoming packet** or **downloading in reference to anything**. Limitations, "prior to reading" (without "said" or "the") **is not limited to prior to reading a pointer for the first parameter within the incoming packet,** which the Appellant is very much concerned.

Response to the argument 2: **Appellant's assertions**, "Ogawa does not disclose or suggest downloading taking place prior to the alleged reading of the of the TCP object pointer for a first pointer", **is misleading** because the prosecution history of this case clearly shows that **no one** including the Examiner has mentioned or **asserted** about downloading taking place prior to the alleged reading of the of the TCP object pointer for a first pointer, which is **not relevant** with the claimed invention and the **claimed limitations** of the claim 3 **are not limited to** usage of **a particular protocol** like **TCP, MAC** etc and whether or not the downloading taking place prior to the alleged reading of the of the TCP object pointer for a first pointer, which the Appellant is very much concerned.

Thus, downloading the offset, the length, and the pointer prior to reading is clearly understood and based on the presented evidence as taught by the reference and interpreted by the Examiner, these limitations as claimed are indeed not novel and hence the rejection should be maintained.

First Ground of Rejection (6) (pages 20 through 22 of the appeal brief)

Claims 4 and 6 (Note: pages 20 through 22 of the appeal brief that represent first ground of rejection (6) for claims 4 and 6 **do not contain any arguments** regarding claimed **limitations of the dependent claim 6)**

Appellant's arguments (regarding claim 4):

(1), "Ogawa does not disclose or suggest explicitly or inherently a step **for routing the first parameter to a peripheral block identified by the pointer prior to processing** as presently claimed"

(2) "Ogawa does not disclose or suggest **prior to processing the first parameter**"

(3) "Ogawa does not appear to discuss routing an unidentified MAC header data element to an unidentified peripheral block identified by the TCP object pointer"

(4) "Ogawa does not disclose or suggest explicitly or inherently wherein the peripheral blocks perform the processing"

(5) "Contrary to the **assertion by the Examiner** Ogawa does not appear to discuss a peripheral block processing an unidentified MAC header data element"

Examiner's response:

The Examiner respectfully disagrees in response to Appellant's arguments.

The Examiner would like to reveal Ogawa's teachings as follows **in response to the Appellant's arguments**:

Response to the argument 1: Ogawa's teachings and disclosure demonstrate **routing** (e.g., usage of bridge, col., 5, lines 11 – 15, also usage of bridging between two networks, usage

of gateway, router, also inherent limitations of WAN, col., 1, line 61 – col., 2, line 29) **said first parameter a peripheral block identified by said pointer prior to (without "the" or "said") processing** (e.g., col., 3, lines 44 – 65, col., 1, line 61 – col., 2, line 29),

Response to the argument 4: wherein the peripheral blocks perform said processing (e.g., lines 44 - 60, col., 4, col., 1, line 61 – col., 2, line 29).

Response to the argument 2: In response to Appellant's argument that the references fail to show certain features of Appellant's invention, it is noted that the features upon which Appellant relies, "**prior to processing the first parameter**", are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). The First inquiry must be into exactly what the claims define. See *In re Wilder*, 166 USPQ 545, 548 (CCPA 1970),

Response to the argument 3: **Appellant's assertions**, "Ogawa does not appear to discuss routing an unidentified MAC header data element to an unidentified peripheral block identified by the TCP object pointer **is misleading** because the prosecution history of this case clearly shows that **no one** including the Examiner has mentioned or **asserted** about routing an unidentified MAC header data element to an unidentified peripheral block identified by the TCP object pointer, which is **not relevant** with the claimed invention and the **claimed limitations** of the claim 4 **are not limited to** whether or not the routing an unidentified MAC header data element to an unidentified peripheral block is identified by the TCP object pointer, which the Appellant is very much concerned.

Response to the argument 5: **Appellant's assertions**, "Ogawa does not appear to discuss a peripheral block processing an unidentified MAC header data element" **is misleading** because the prosecution history of this case clearly shows that **no one** including the Examiner has mentioned or **asserted** about peripheral block processing an unidentified MAC header data element, which is **not relevant** with the claimed invention and the **claimed limitations** of the claim 4 **are not limited to** whether or not the peripheral block processing an unidentified MAC header data element, which the Appellant is very much concerned.

Further, **contrary to Appellant's assertions**, limitations, "prior to processing" (without "said" or "the") **is not limited** to **prior to processing the first parameter in accordance with the pointer to produce a second parameter,** limitations, "at least one of a plurality of peripheral blocks identified by the pointer" **is not limited** to **plurality of peripheral blocks identified by the pointer,** which the Appellant is very much concerned.

Thus, routing the first parameter to a peripheral block identified by the pointer prior to processing, wherein the peripheral blocks perform the processing is clearly understood and based on the presented evidence as taught by the reference and interpreted by the Examiner, these limitations as claimed are indeed not novel and hence the rejection should be maintained.

First Ground of Rejection (7) (pages 22 through 23 of the appeal brief)

Claim 5

Appellant's arguments (regarding claim 5):

(1), "Ogawa does not disclose or suggest explicitly or inherently a step **for reading a second offset and a second length for a second network protocol prior to assembling an outgoing packet** as presently claimed"

Examiner's response:

The Examiner respectfully disagrees in response to Appellant's arguments.

The Examiner would like to reveal Ogawa's teachings as follows **in response to the Appellant's arguments**:

Response to the argument 1: Ogawa's teachings and disclosure demonstrate

a step **for reading a second offset and a second length** (e.g., another offset/flag, length, col., 13, lines 50 –55, reading another offset having inherent index / position, figure 21, packet type, figure 23) **for a second network protocol** (e.g., another protocol used by the second network, col., 7, lines 54 – 58, e.g., lines 19 - 67, page 10, e.g., col., 5, lines 11 – 15, also usage of bridging between two networks, usage of bridge, gateway, router, also inherent limitations of WAN, col., 1, line 61 – col., 2, line 29) **prior to assembling the outgoing packet** (see figure 21 containing iteration for 12^{th} iteration, 14^{th} iteration etc for assembling, the assembling performed after the reading is performed to read the second offset and the second length because the second offset and the second length is used and needed for assembling, e.g., lines 19 - 67, page 10, col., 8, lines 50 – 63).

Further, **contrary to Appellant's assertions**, limitations, "reading a second offset and a second length" (without "said" or "the") **is not limited** to **reading a second offset and a second length for the first parameter in accordance with the pointer to produce a second parameter** or **reading a second offset and a second length from the incoming packet,**

limitations, "a second network protocol" **is not limited** to **a second network protocol for the second parameter for the second network,** limitations, "a second network protocol" **is not limited** to **a second network protocol for the second parameter for the second network,** which the Appellant is very much concerned.

Thus, the step of reading a second offset and a second length for a second network protocol prior to assembling the outgoing packet is clearly understood and based on the presented evidence as taught by the reference and interpreted by the Examiner, these limitations as claimed are indeed not novel and hence the rejection should be maintained.

First Ground of Rejection (8) (pages 24 through 25 of the appeal brief)

Claim 7

Appellant's arguments (regarding claim 7):

(1), "Ogawa does not disclose or suggest explicitly or inherently step (B) of claim 1 is **at least two processes** of a content addressable memory process, a protocol identification analysis process, a buffer process, a counter process, a parameter discard process, a content addressable memory process, a time to live process, comparison process, counter process, a value swapping process, a stuffing process, cyclic redundancy a de-stuffing process, checksum process, a parity process, a first-in- first-out process, a length construction generator header error control synchronization process, a frame relay lookup process, data link connection identifier process, protocol identification analysis process, point-to-point protocol verification process, parameter discard process, and a buffer process as presently claimed".

(2) "Ogawa does not appear to disclose processes to operate on an unidentified MAC header data element"

Examiner's response:

The Examiner respectfully disagrees in response to Appellant's arguments.

The Examiner would like to reveal Ogawa's teachings as follows **in response to the Appellant's arguments**:

Response to the argument 1: Ogawa's teachings and disclosure demonstrate that step (B) of claim 1 is **at least two processes** of a (1) **content addressable memory process** (e.g., col., 4, lines 45 – 60 containing process for CAM (contents addressable Memory) col., 3, line 60 – col., 4, line 11), a (2) **protocol identification analysis process** (e.g., process for identifying a protocol type of each protocol hierarchy from the protocol type code, col., 3, line 55 – col., 4, line 11), (3) **a counter process** (e.g., process for counter, col., 4, lines 23 – 29, col., 3, line 55 – col., 4, line 11), (4) **a buffer process**, (e.g., process of RAM, inherent buffer, col., 4, lines 55 – 60, col., 3, line 55 – col., 4, line 11), (Note: **more than two processes are identified in** the cited reference **Ogawa** to meet the claim) a parameter discard process, a content addressable memory process, a time to live process, comparison process, counter process, a value swapping process, a stuffing process, cyclic redundancy a de-stuffing process, checksum process, a parity process, a first-in- first-out process, a length construction generator header error control synchronization process, a frame relay lookup process, data link connection identifier process, protocol identification analysis process, point-to-point protocol verification process, parameter discard process, and a buffer process (e.g., col., 3, line 12 – col., 4, lines 64) as presently claimed".

Response to the argument 2: **Appellant's assertions**, "Ogawa does not appear to disclose processes to operate on an unidentified MAC header data element" **is misleading** because the prosecution history of this case clearly shows that **no one** including the Examiner has mentioned or **asserted** about processes to operate on an unidentified MAC header data element, which is **not relevant** with the claimed invention and the **claimed limitations** of the claim 7 **are not limited to** whether or not processes operate on an unidentified MAC header data element, which the Appellant is very much concerned.

Thus, step (B) of claim 1 is at least two processes of the claim 7 is clearly understood and based on the presented evidence as taught by the reference and interpreted by the Examiner, these limitations as claimed are indeed not novel and hence the rejection should be maintained.

First Ground of Rejection (9) (pages 25 through 26 of the appeal brief)

Claim 11

Appellant's arguments (regarding claim 11):

(1), "Ogawa does not disclose or suggest explicitly or inherently **selecting among a plurality of frame delineation method for a plurality of network protocols prior to delineating** as presently claimed".

Examiner's response:

The Examiner respectfully disagrees in response to Appellant's arguments.

The Examiner would like to reveal Ogawa's teachings as follows **in response to the Appellant's arguments**:

Response to the argument 1: Ogawa's teachings and disclosure demonstrate a step of **selecting among plurality of frame delineation methods** (e.g. frame end detection, header end timing detection, protocol recognition, etc., col., 4, lines 19 – 43, figure 12 performing frame delineation, **for a plurality of network protocols** (e.g. depending on each protocol of each different protocol hierarchy, col., 3, lines 1 – 9) **prior to delineating** (e.g., delineating method is applied for the network protocol specific and the delineating is performed after the selection of the delineating method because delineating would not be performed without delineating method, col., 4, lines 19 – 43, line 54, col., 7 - line 12, col., 8).

Thus, selecting among a plurality of frame delineation methods for a plurality of network protocols prior to delineating is clearly understood and based on the presented evidence as taught by the reference and interpreted by the Examiner, these limitations as claimed are indeed not novel and hence the rejection should be maintained.

First Ground of Rejection (10) (pages 26 through 27 of the appeal brief)

Claim 13

Appellant's arguments (regarding claim 13):

(1) "Ogawa does not disclose or suggest explicitly or inherently a step of **framing the outgoing packet to produce a transmit frame for said second network in response to presenting said outgoing packet** as presently claimed".

(2) "An ability to receive an incoming packet does not expressly or inherently suggest an ability to frame an outgoing packet".

(3) "Ogawa does not appear to have an ability to frame an outgoing packet".

Examiner's response:

The Examiner respectfully disagrees in response to Appellant's arguments.

The Examiner would like to reveal Ogawa's teachings as follows **in response to the Appellant's arguments**:

Response to the argument 1: Ogawa's teachings and disclosure demonstrate **framing the outgoing packet** (e.g., adding information to the packet being built for outgoing, col., 4, lines 3 – 12, col., 4, lines 45 – 54, usage of queue / memory for output port, figure 27, also, iterations of building outgoing packet information is shown in figures 24, 25, creation of packet information including pay-load information based on protocol used, col., 19, lines 25 - 29) **to produce a transmit frame** (e.g., col., lines 2 – 4) **for said second network** (e.g., another network, col., 5, lines 11 – 15, e.g., use of internetwork repeater between first and second networks, col., 12, lines 41 – 49, col., 2, lines 5 – 14) **in response to presenting said outgoing packet** (e.g., adding information to the packet being built for outgoing, col., 4, lines 3 – 12, col., 4, lines 45 - 54). Further, contrary to Appellant's assertions, limitations, "outgoing packet" **is not limited** to a packet outgoing from the circuit or database etc, as the claimed invention does not specify outgoing in reference to anything. Limitations, "present an outgoing packet" **is not limited to** generating or producing, etc., of an outgoing packet. **In fact**, the Appellant's provided Appendix A, pages A- 3 to5 (dated 1998) of the appeal brief clearly **also** supports (**provide more evidence**) for these limitations.

Response to the argument 2: **Appellant's assertions**, "An ability to receive an incoming packet does not expressly or inherently suggest an ability to frame an outgoing packet" **is misleading** because the prosecution history of this case clearly shows that **no one** including the

Examiner has mentioned or **asserted** about an ability to receive an incoming packet does not expressly or inherently suggest an ability to frame an outgoing packet, which is **not relevant** with the claimed invention and the **claimed limitations** of the claim 13 **are not limited to** whether or not an ability to receive an incoming packet expressly or inherently suggest an ability to frame an outgoing packet, which the Appellant is very much concerned.

Response to the argument 3: Ogawa clearly discloses **to frame an outgoing packet** (e.g., adding information to the packet being built for outgoing, col., 4, lines 3 – 12, col., 4, lines 45 – 54, usage of queue / memory for output port, figure 27, also, iterations of building outgoing packet information is shown in figures 24, 25, creation of packet information including pay-load information based on protocol used, col., 19, lines 25 - 29).

Thus, the step of framing the outgoing packet to produce a transmit frame for the second network in response to presenting the outgoing packet is clearly understood and based on the presented evidence as taught by the reference and interpreted by the Examiner, these limitations as claimed are indeed not novel and hence the rejection should be maintained.

First Ground of Rejection (11) (pages 28 through 29 of the appeal brief)

Claims 14 and 15 (Note: pages 28 to 29 of the appeal brief that represent first ground of rejection (11) for claims 14 and 15 **do not contain any arguments** regarding claimed **limitations of the dependent claim 15**)

Appellant's arguments (regarding claim 14):

(1) "Ogawa does not disclose or suggest explicitly or inherently a step of **selecting among a plurality of framing methods for a plurality of network protocols prior to framing**"

(2) "Ogawa states that the sequencer is part of a first embodiment and figure 1 is a block diagram showing the structure of a first embodiment of a data receiving device and one of ordinary skilled in the art would appear to understand receiving devices deframe incoming information, not select among multiple framing methods for transmitting information".

Examiner's response:

The Examiner respectfully disagrees in response to Appellant's arguments.

The Examiner would like to reveal Ogawa's teachings as follows **in response to the Appellant's arguments**:

Response to the argument 1: Ogawa's teachings and disclosure demonstrate a step of **selecting among a plurality of framing methods** (e.g., creation of frame / packet information including pay-load information based on protocol used, col., 19, lines 25 – 29, selecting protocol specific framing method for adding information to the frame / packet being built for outgoing, col., 4, lines 3 – 12, col., 4, lines 45 – 54, usage of queue / memory for output port, figure 27, also, iterations of building outgoing frame / packet information is shown in figures 24, 25,) **for a plurality of network protocols** (e.g. depending on each protocol of each different protocol hierarchy, col., 3, lines 1 – 9) **prior to framing** (e.g., framing method is applied for the network protocol specific and the framing is performed after the selection of the framing method because framing would not be performed without framing method, col., 4, lines 19 – 43, line 54, col., 7 - line 12, col., 8). Further, contrary to Appellant's assertions, limitations, "framing" **is not limited**

to **framing for a packet outgoing from the circuit or database** etc, as the claimed invention does not specify framing in reference to anything. Limitations, "selection among a plurality of framing methods" **is not limited to selection among a plurality of framing methods for an outgoing packet**. **In fact**, the Appellant's provided Appendix A, pages A- 3 to5 (dated 1998) of the appeal brief clearly **also** supports (**provide more evidence**) for these limitations.

Response to the argument 2: **Appellant's assertions**, "Ogawa states that the sequencer is part of a first embodiment and figure 1 is a block diagram showing the structure of a first embodiment of a data receiving device and one of ordinary skilled in the art would appear to understand receiving devices deframe incoming information, not select among multiple framing methods for transmitting information" **is misleading** because the prosecution history of this case clearly shows that **no one** including the Examiner has mentioned or **asserted** about one of ordinary skilled in the art would appear to understand receiving devices deframe incoming information equivalent to selection among multiple framing methods for transmitting information, which is **not relevant** with the claimed invention and the **claimed limitations** of the claim 13 **are not limited to** whether or not one of ordinary skilled in the art would appear to understand receiving devices deframe incoming information equivalent to selection among multiple framing methods for transmitting information, which the Appellant is very much concerned.

Thus, the step of selecting among a plurality of framing methods for a plurality of network protocols prior to framing is clearly understood and based on the presented evidence as taught by the reference and interpreted by the Examiner, these limitations as claimed are indeed not novel and hence the rejection should be maintained.

Second Ground of Rejection (1) (pages 26 through 31 of the appeal brief)

Claim 9

Appellant's arguments (regarding claim 9):

(1) "The Examiner bears the initial burden of factually supporting prima facie conclusion of obviousness"

(2) "The Examiner must show that there is some suggestion or motivation to modify or combine the references"

(3) "The Examiner must show reasonable expectation of success"

(4) "The Examiner must not merely use Appellant's disclosure for the suggestion to modify and the reasonable expectation success"

(5) "The Examiner fails to establish a clear and particular showing of a teaching or motivation to modify Ogawa to make processing of the first parameter non-programmable"

(6) "The alleged motivations by the Examiner are not credited to any reference or knowledge generally available to one of ordinary skill"

(7) "The alleged motivations are not credited to the nature of the problem to be solved"

(8) "The alleged motivations are not based on objective evidence of record"

(9) "The alleged motivations are merely conclusory statements lacking the required supporting evidence"

(10) "The fact that Yusa U. S. Patent No. 5,633,806 teaches a concept does not explain why one of ordinary skill in the art would be motivated to modify Ogawa with that concept"

Examiner's response:

The Examiner respectfully disagrees in response to Appellant's arguments.

Response to the arguments 1 through 10:

As per claim 9, Ogawa teaches **processing said first parameter** (e.g., parameter of the received frame, col., 11, lines 58 – 67, col., 13, lines 15 – 21, header parameter, protocol information, length information, destination network address, frame length, destination port number, source network address, source port number, col., 8, lines 1 – 18, packet type, figure 23, header length, protocol information, col., 13, lines 24 – 29, parameter having a data length of certain number of bits, destination and source socket numbers, col., 18, lines 19 - 42)

However, Ogawa does not specifically mention about step (B) being non-programmable. "Official Notice" is taken that both the concept and advantages of providing step (B) being non-programmable is well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the concept of making the processing non-programmable with the teaching's of Ogawa in order to facilitate non-programmable processing for the step (B) because **at least one of the motivations** is that the concept of non-programmable processing would enhance processing the steps taught by the Ogawa. The usage of non-programmable circuit design would help **increase** the degree of freedom of circuit design.

For example, Yusa et al., 5,633,806, 1997, clearly discloses the **well-known concept** of **non-programmable processing** (e.g., use of fixed function in the core region, col., 14, lines 6 – 21). The usage of non-programmable circuit design would help increase the degree of freedom of circuit design (**please see evidence** abstract of the Yusa et al., 5,633,806, 1997).

The claimed invention, **please see claim 1 step (B), does not provide** anything for the processing. **One of ordinary skill in the art at the time the invention** was made **very well knows** that **something is needed to implement** the processing. In order to do the processing, the **Ogawa discloses** usage of **several alternatives** and Ogawa further mentions that the **modifications** to his invention are possible and are **also within its true scope of the invention** (e.g., **please see evidence**, Ogawa, col., 21, lines 1-2).

Yusa et al., 5,633,806, 1997, not only discloses the well-known concept of non-programmable processing (e.g., use of fixed function in the core region, col., 14, lines 6 – 21) **but also** discloses **at least one of the benefits** of the non-programmable processing, i.e., the usage of non-programmable circuit design would help increase the degree of freedom of circuit design (**please see evidence** abstract of the Yusa et al., 5,633,806, 1997).

Since, processing of step (B) **needs to implemented** and the Yusa's teaching of the concept of non-programmable **use for implementation** is available to **one of ordinary skill in the art at the time the invention** was made, the one of ordinary skill in the art at the time the invention would be tempted to utilize the concept of the non-programmable for the implementation.

Also, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of a primary reference. It is also not that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinally skill in the art. *In re Keller*, 642 F.2d 414, 425, 208 USPQ 871, 881 (CCPA 1981); *In re Young*, 927 F.2d 588, 591, 18 USPQ2d 1089, 1091 (Fed. Cir. 1991), and the reason or motivation to modify the

reference may often suggest what the inventor has done, but for a different purpose or to solve a different problem. It is not necessary that the prior art suggest the combination to achieve the same advantage or result discovered by applicant. *In re Linter*, 458 F.2d 1013, 173 USPQ 560 (CCPA 1972). There is no requirement that the prior art provide the same reason as the applicant to make the claimed invention. *Ex parte Levengood*, 28 USPQ2d 1300, 1302 (Bd. Pat. App. & Inter. 1993). Further, in response to applicant's argument that the Examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

In fact, the Appellant is trying to accomplish **just** a method of bridging an incoming packet from a first network to a second network (e.g., col., 5, lines 11 – 15), which the Ogawa references clearly teaches. The **claimed invention does not provide the benefit** of using the non-programmable. The **claimed invention does not provide how** the non-programmable is implemented differently than the well-known teachings including the cited references. The **Appellant did not provide** evidence on **why** the well-known teachings including the cited references are not combinable. The **Appellant did not provide** evidence on **how** the claimed invention is implemented **differently then the well-known teachings** including the cited references.

Thus, the Examiner acknowledges that the initial burden of factually supporting prima facie conclusion of obviousness has been properly meet; the Examiner acknowledges that there is a suggestion or motivation to modify or combine the cited references; the Examiner acknowledges that reasonable expectation of success is demonstrated; the Examiner acknowledges that based on the evidence provided the suggestion to modify and the reasonable expectation success are properly presented and not merely used Appellant's disclosure; the Examiner acknowledges that **a clear and particular showing** of a teaching or motivation to modify Ogawa is properly **established to make processing of the first parameter** non-programmable; the Examiner acknowledges that the motivations **are credited** to the cited references or knowledge generally available to one of ordinary skilled in the art; the Examiner acknowledges that the motivations **are to the nature** of the problem to be solved (something needed to perform the processing of step (B) of claim 1); the Examiner acknowledges that the motivations **are based** on objective evidence of record; the Examiner acknowledges that the motivations are **not** merely conclusory statements lacking the required supporting evidence (**please see evidence** abstract, col., 14, 6-21 lines of the Yusa et al., 5,633,806, 1997 for additional motivations and advantages of using them).

Thus, the step (B) is non-programmable is clearly understood and based on the presented evidence as taught by the reference and interpreted by the Examiner, these limitations as claimed are indeed not novel and hence the rejection should be maintained.

Third Ground of Rejection (2) (pages 32 through 35 of the appeal brief) (Note: please page 32 line 1 that does not contain Third Ground of Rejection "(1)" versus page 6, line 1 mentioning about claims 18-20 under the Third Ground of Rejection)

Claim 18

Appellant's arguments (regarding claim 18):

(1) "the combined teachings of the cited references do not disclose or suggest means for processing the first parameter comprises a plurality of peripheral means **at least one (i) linked to the pointer and (ii) configured to perform a process involving the first parameter**".

(2) "Nowhere Wilford appears to discuss **modules of memory processing information including header** as alleged by the Examiner"

(3) "The Examiner has not provide any explanation or evidence that one of ordinary skill in the art would understand how to combine and/or modify the MAC header data of Ogawa and the information including header to create some undefined first parameter within an incoming packet"

(4) "The Examiner has not provided an evidence on how to combine the TCP pointer of Ogawa with the concept of TAG usage"

(5) "The Examiner has not provided any evidence on how to combine the modules of memory to be linked to the undefined pointer"

(6) "The Examiner has not provided any evidence on how to combine the modules of memory to perform a process on the undefined first parameter"

(7) "The Examiner has not provided any evidence on how to combine the modules of memory to be linked to the undefined pointer"

(8) "The Examiner bears the initial burden of factually supporting prima facie conclusion of obviousness"

(9) "The Examiner must show that there is some suggestion or motivation to modify or combine the references"

(10) "The Examiner must show reasonable expectation of success"

(11) "The Examiner must not merely use Appellant's disclosure for the suggestion to modify and the reasonable expectation success"

(12) "The alleged motivations by the Examiner are not credited to any reference or knowledge generally available to one of ordinary skill"

(13) "The alleged motivations are not credited to the nature of the problem to be solved"

(14) "The alleged motivations are not based on objective evidence of record"

(15) "The alleged motivations are merely conclusory statements lacking the required supporting evidence"

Examiner's response:

The Examiner respectfully disagrees in response to Appellant's arguments.

First, the **claim 18 has been objected to, which the Appellant did not address at all**. Please see claimed limitations of the claim 7, which contain "**at least two** a point-to-point protocol verification process, a parameter discard process **and** a buffer process" (**broadly interpreted as "at least two",** similar to limitations of the claim 4, which contain "**at least one of a plurality blocks**", (**broadly interpreted as "at least one")**, which is **similar to** the **at least one (i)** linked to the pointer **and (ii)** configured to perform a process involving the first parameter. **Hence, either (i) or (ii)** only (**one, broadly interpreted as "at least one"**) exist in

the claim 18). Also, the dependent claim 18 **only contains a plurality of peripherals** and **either (i) or (ii),** and **not other** interpretations as asserted by the Appellant that includes additional interpretation of the limitations **compared to what is claimed**. Note: **The Appellant has presented arguments considering** that both (i) and (ii) exist in the claim 18 and that the plurality of peripheral means perform both (i) and (ii), **contrary to what is claimed** (please see claim 18). In fact, the **claimed limitations of the claim 18** also do **not specifically mention** about **what** or **how** or **when** or **why** or **where** is linked to the pointer and **what** or **how** or **when** or **why** or **where** is configured to perform a process involving the first parameter.

Response to the argument 2: **Appellant's assertions**, "Nowhere Wilford appears to discuss **modules of memory processing information including header** as alleged by the Examiner" **is misleading** because the prosecution history of this case clearly shows that **no one** including the Examiner has mentioned or **asserted** about **modules of memory processing information including header**, which is **not relevant or necessary for combining the concerned teachings** with the claimed invention and the **claimed limitations** of the claim 18 **are not limited to** whether or not **modules of memory processing information including header**, which the Appellant is very much concerned.

Response to the argument 3: **Appellant's assertions**, "The Examiner has not provide any explanation or evidence that one of ordinary skill in the art would understand how to combine and/or modify the MAC header data of Ogawa and the information including header to create some undefined first parameter within an incoming packet" **is misleading** because the prosecution history of this case clearly shows that **no one** including the Examiner has mentioned or **asserted** about one of ordinary skill in the art would understand how to combine and/or

modify the MAC header data of Ogawa and the information including header to create some undefined first parameter within an incoming packet, which is **not relevant or necessary for combining the concerned teachings** with the claimed invention and the **claimed limitations** of the claim 18 **are not limited to** whether or not one of ordinary skill in the art would understand how to combine and/or modify the MAC header data of Ogawa and the information including header to create some undefined first parameter within an incoming packet, which the Appellant is very much concerned.

Response to the argument 4: **Appellant's assertions**, "The Examiner has not provided an evidence on how to combine the TCP pointer of Ogawa with the concept of TAG usage" **is misleading** because the prosecution history of this case clearly shows that **no one** including the Examiner has mentioned or **asserted** an evidence on how to combine the TCP pointer of Ogawa with the concept of TAG usage, which is **not relevant or necessary for combining the concerned teachings** with the claimed invention and the **claimed limitations** of the claim 18 **are not limited to** whether or not how to combine the TCP pointer of Ogawa with the concept of TAG usage, which the Appellant is very much concerned.

Response to the argument 5: **Appellant's assertions**, "The Examiner has not provided any evidence on how to combine the modules of memory to be linked to the undefined pointer" **is misleading** because the prosecution history of this case clearly shows that **no one** including the Examiner has mentioned or **asserted** how to combine the modules of memory to be linked to the undefined pointer, which is **not relevant or necessary for combining the concerned teachings** with the claimed invention and the **claimed limitations** of the claim 18 **are not**

limited to whether or not how to combine the modules of memory to be linked to the undefined pointer, which the Appellant is very much concerned.

Response to the argument 6: **Appellant's assertions**, "The Examiner has not provided any evidence on how to combine the modules of memory to perform a process on the undefined first parameter" **is misleading** because the prosecution history of this case clearly shows that **no one** including the Examiner has mentioned or **asserted** how to combine the modules of memory to perform a process on the undefined first parameter, which is **not relevant or necessary for combining the concerned teachings** with the claimed invention and the **claimed limitations** of the claim 18 **are not limited to** whether or not how to how to combine the modules of memory . to perform a process on the undefined first parameter, which the Appellant is very much concerned.

Response to the argument 7: **Appellant's assertions**, "The Examiner has not provided any evidence on how to combine the modules of memory to be linked to the undefined pointer" **is misleading** because the prosecution history of this case clearly shows that **no one** including the Examiner has mentioned or **asserted** to combine the modules of memory to be linked to the undefined pointer, which is **not relevant or necessary for combining the concerned teachings** with the claimed invention and the **claimed limitations** of the claim 18 **are not limited to** whether or not to combine the modules of memory to be linked to the undefined pointer, which the Appellant is very much concerned.

Response to the arguments 1, 8 through 15:

As per claim 18, Ogawa teaches **concept of usage of peripherals** (please see col., 4, lines 45 – 60, col., 4, lines 31 – 36) **pointers**, (e.g., parameter of the received frame, col., 11,

lines 58 – 67, col., 13, lines 15 – 21, header parameter, protocol information, length information, destination network address, frame length, destination port number, source network address, source port number, col., 8, lines 1 – 18, packet type, figure 23, header length, protocol information, col., 13, lines 24 – 29, parameter having a data length of certain number of bits, destination and source socket numbers, col., 18, lines 19 - 42) **process involving the first parameter** (e.g., parameter of the received frame, col., 11, lines 58 – 67, lines 27 - 65, col., 9).

To make better understanding the Examiner **further cited reference Wilford** that discloses **a plurality of peripheral means** (e.g., use of modules of memory and/or memory controller that does processing and support the functionality, figures 9, 10, 15, 26) **at least one (i)** linked to the pointer (e.g., concept of TAG etc pointer equivalent usage, col., 49, lines 15 – 38) **(ii)** configured to perform a process (e.g., perform handling information, col., 6, lines 2 – 23) involving the first parameter (e.g., parameter of the received frame, col., 11, lines 58 – 67 etc., col., 5, lines 36 – 51). Note: Examiner would also like to point out that **Wilford is a pertinent reference for the claimed invention including almost all the claimed invention of the claims** (please refer to it's figures 11-14 and its related description that also discloses what the Ogawa teaches regarding other claims, for example, **Wilford also teaches interfacing to different networks, (e.g., col., 4, lines 46 – 65) de-framing etc using parameter, pointer etc (e.g., col., 2, lines 55 – 67) in compliance with a plurality of network protocols (e.g., col., 4, lines 46 – 65).**

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Ogawa with the teachings of Wilford in order to facilitate usage of a plurality of peripherals means because **at least one of the motivations** is that the

peripherals would provide enhancing the handling the information associated with the pointer and the parameter information would help the software to **process information for the circuit** (please see col., 11, lines 58 – 67 etc., col., 5, lines 36 – 51 of Wilford for the further teachings and the advantages and benefits of the peripherals).

The claimed invention, **please see claim 16, does not provide** anything for the processing. **One of ordinary skill in the art at the time the invention** was made **very well knows** that **something is needed to implement** the processing. In order to do the processing, the **Ogawa discloses** usage of **several alternatives** and Ogawa further mentions that the **modifications** to his invention are possible and are **also within its true scope of the invention** (e.g., **please see evidence**, Ogawa, col., 21, lines 1-2).

Wilford, not only discloses the well-known concept of using the peripherals and something linked to the pointer **or** configured to perform a process involving the first parameter (e.g., peripherals supporting parameter of the received frame, etc., col., 11, lines 58 – 67, lines 27 - 65, col., 9) **but also** discloses **at least one of the benefits** of it (**please see evidence** col., 11, lines 58 – 67, lines 27 - 65, col., 9).

Since, processing **needs to implemented** and the **Wilford**'s teachings of the concept of peripheral means etc is available to **one of ordinary skill in the art at the time the invention** was made, and the one of ordinary skill in the art at the time the invention would be tempted to utilize the concept of the peripheral means etc provided by the Wilford.

Also, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of a primary reference. It is also not that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what

the combined teachings of the references would have suggested to those of ordinally skill in the art. *In re Keller*, 642 F.2d 414, 425, 208 USPQ 871, 881 (CCPA 1981); *In re Young*, 927 F.2d 588, 591, 18 USPQ2d 1089, 1091 (Fed. Cir. 1991), and the reason or motivation to modify the reference may often suggest what the inventor has done, but for a different purpose or to solve a different problem. It is not necessary that the prior art suggest the combination to achieve the same advantage or result discovered by applicant. *In re Linter*, 458 F.2d 1013, 173 USPQ 560 (CCPA 1972). There is no requirement that the prior art provide the same reason as the applicant to make the claimed invention. *Ex parte Levengood*, 28 USPQ2d 1300, 1302 (Bd. Pat. App. & Inter. 1993). Further, in response to applicant's argument that the Examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

Note: The **Appellant's assertions** that the claimed invention has **a circuit (single) further comprising plurality of peripheral means** along with **three circuit means** for reading, processing and presenting (please see claim 18) **contradicts** with the another **Appellant's assertions** that the figure 2 which is part of the specification of the application under prosecution discloses **an assembly (102)** (not a single circuit as claimed) **further comprising plurality of peripheral means** along with three circuit means for reading, processing and presenting.

In fact, the claimed invention **does not provide support** on how the **further plurality of peripheral means** along with three circuit means for reading, processing and presenting are **different from each other** and **why and what is that** the same circuit cannot implement limitations of other means. The claimed invention also **do not support on how** the claimed **circuits are different** than the well known circuits including the circuits cited by the references.

The Appellant is trying to accomplish **just** a method of bridging an incoming packet from a first network to a second network (e.g., col., 5, lines 11 – 15), which the Ogawa references clearly teaches. The **claimed invention (see claim 18) does not provide the benefit** of using the peripherals or linking to the pointer **or** perform a process involving the first parameter. The **claimed invention does not provide what** or **how** or **when** or **why** or **where** the linked to the pointer or configured to perform a process is implemented differently than the well-known teachings including the cited references. The **Appellant did not provide** evidence on **why** the well-known teachings including the cited references are not combinable. The **Appellant did not provide** evidence on **how** the claimed invention is implemented **differently then the well-known teachings** including the cited references.

Thus, the Examiner acknowledges that the initial burden of factually supporting prima facie conclusion of obviousness has been properly meet; the Examiner acknowledges that there is a suggestion or motivation to modify or combine the cited references; the Examiner acknowledges that reasonable expectation of success is demonstrated; the Examiner acknowledges that based on the evidence provided the suggestion to modify and the reasonable expectation success are properly presented and not merely used Appellant's disclosure; the Examiner acknowledges that **a clear and particular showing** of a teaching or motivation to

modify Ogawa is properly **established for means for processing comprising a plurality of peripheral means and at least one of (i) linked to said pointer and (ii) configured to perform a process involving the first parameter**; the Examiner acknowledges that the motivations **are credited** to the cited references and/or knowledge generally available to one of ordinary skilled in the art; the Examiner acknowledges that the motivations **are to the nature** of the problem to be solved (something needed to perform the processing of claim 18); the Examiner acknowledges that the motivations **are based** on objective evidence of record; the Examiner acknowledges that the motivations are **not** merely conclusory statements lacking the required supporting evidence (**please see evidence** abstract, col., 11, lines 58 – 67, lines 27 - 65, col., 9 of the Wilford for additional motivations and advantages of using them).

Thus, wherein the means for processing further comprises a plurality of peripheral means at least one (i) linked to the pointer and (ii) configured to perform a process involving the first parameter, as claimed is clearly understood and based on the presented evidence as taught by the reference and interpreted by the Examiner, these limitations as claimed are indeed not novel and hence the rejection should be maintained.

Third Ground of Rejection (3) (pages 35 through 36 of the appeal brief)

Claims 19 and 20 (Note: pages 35 through 36 of the appeal brief that represent Third Ground of Rejection (3) for claims 19 and 20 **do not contain any arguments** regarding claimed **limitations of the dependent claim 20)**

Appellant's arguments (regarding claim 19) (Note: line 5, page 35 of the appeal brief, seems to have type error and the "claims 18 and 20" should be "19 and 20", as the line 6, of the same page contains properly argued "19 and 20"):

(1) "The Examiner fails to identify any circuit in either Ogawa or Wilford similar to the claimed means for processing the first parameter"

(2) "the combined teachings of the cited references do not disclose or suggest the **peripheral means comprises a first plurality of the peripheral means internal to the means for processing and a second plurality of the peripheral means external to the means for processing**".

(3) "The Examiner fails to establish that the external memory of Wilford is in fact external to a circuit similar to the claimed means for processing a first parameter"

(4) "The Examiner fails to establish that the internal memory of Wilford is in fact internal to a circuit similar to the claimed means for processing a first parameter"

(5) "The means for processing appears to be improperly based on the claimed language, not on some combination and/or modification that one of ordinary skill in the art would be motivated to make or find obvious"

(6) "Prima facie obviousness has not been established for lack of evidence that the references teach all of the claim"

Examiner's response:

The Examiner respectfully disagrees in response to Appellant's arguments.

First, the **claim 18 has been objected to, which the Appellant did not address at all**. **Since, claims 19 and 20 are dependent claims of 18,** similar objections applies to the claims 19 and 20 as mentioned in the Third Ground of Rejection (2).

Response to the argument 1: Ogawa clearly teaches **claimed means for** (e.g., circuits of abstract, circuits of figure 1, col., 3, lines 44 – 59, usage of bridge, col., 5, lines 11 – 15, also usage of bridging between two networks, usage of gateway, router, the router components that is similar to the application under prosecution that contains the brief summary of invention and the specification mentioning usage of router and components, also use of WAN that contain circuits to do processing etc, col., 1, line 61 – col., 2, line 29) **processing said first parameter** (e.g., parameter of the received frame, col., 11, lines 58 – 67, col., 13, lines 15 – 21, header parameter, protocol information, length information, destination network address, frame length, destination port number, source network address, source port number, col., 8, lines 1 – 18, packet type, figure 23, header length, protocol information, col., 13, lines 24 – 29, parameter having a data length of certain number of bits, destination and source socket numbers, col., 18, lines 19 - 42). **In fact, Wilford also teaches claimed means** (e.g., col., 4, lines 46 – 65, e.g., col., 2, lines 55 – 67) **for processing said first parameter** (e.g., col., 4, lines 46 – 65, e.g., col., 2, lines 55 – 67).

Response to the arguments 2 to 6: As per claim 18, Ogawa teaches a **concept of usage of peripherals that are internal and external that can be used for processing** (please see col., 4, lines 32 – 60, col., 4, lines 31 – 36) **for the first parameter** (e.g., parameter of the received frame, col., 11, lines 58 – 67, lines 27 - 65, col., 9).

To make better understanding the Examiner **further cited reference Wilford** that discloses and/or teaches **a first plurality** (e.g., use of modules of memory and/or memory controller that are internal and not external, figures 9, 10, 15, 26, col., 48, lines 39 - 58) **of said peripheral means** (e.g., use of modules of memory and/or memory controller, figures 9, 10, 15, 26) **that are internal** (e.g., use of modules of memory and/or memory controller that are internal and not external, figures 9, 10, 15, 26, col., 48, lines 39 - 58) **and a second plurality** (e.g., use of modules of memory and/or memory controller that are external and not internal, figures 9, 10, 15, 26, col., 48, lines 25 - 37) **of said peripheral means** (e.g., use of modules of memory and/or memory controller, figures 9, 10, 15, 26) **that are external** (e.g., use of modules of memory and/or memory controller that are external and not internal, figures 9, 10, 15, 26, col., 48, lines 25 - 37).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Ogawa with the teachings of Wilford in order to facilitate internal and external peripheral means because **at least one of the motivations** is that the internal peripherals would enhance supporting information that is within the processing means, while the external peripherals would enhance supporting information that is outside the processing means (please see col., 11, lines 58 – 67 etc., col., 5, lines 36 – 51 of Wilford for the further teachings and the advantages and benefits of the internal / external peripherals).

The claimed invention, **please see claim 16 to which the claim refers, does not provide** anything for the processing. **One of ordinary skill in the art at the time the invention** was made **very well knows** that **something is needed to implement** the processing. In order to do the processing, the **Ogawa discloses** usage of **several alternatives** and Ogawa further

mentions that the **modifications** to his invention are possible and are **also within its true scope of the invention** (e.g., **please see evidence**, Ogawa, col., 21, lines 1-2).

Wilford, not only discloses the well-known concept of using the internal/ external peripherals (e.g., internal / external peripherals supporting parameter of the received frame, etc., col., 11, lines 58 – 67, lines 27 - 65, col., 9) **but also** discloses **at least one of the benefits** of it (**please see evidence** col., 11, lines 58 – 67, lines 27 - 65, col., 9).

Since, processing **needs to implemented** and the **Wilford**'s teachings of the concept of internal / external peripheral means etc is available to **one of ordinary skill in the art at the time the invention** was made, and the one of ordinary skill in the art at the time the invention would be tempted to utilize the concept of the peripheral means etc provided by the Wilford.

Also, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of a primary reference. It is also not that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinally skill in the art. *In re Keller*, 642 F.2d 414, 425, 208 USPQ 871, 881 (CCPA 1981); *In re Young*, 927 F.2d 588, 591, 18 USPQ2d 1089, 1091 (Fed. Cir. 1991), and the reason or motivation to modify the reference may often suggest what the inventor has done, but for a different purpose or to solve a different problem. It is not necessary that the prior art suggest the combination to achieve the same advantage or result discovered by applicant. *In re Linter*, 458 F.2d 1013, 173 USPQ 560 (CCPA 1972). There is no requirement that the prior art provide the same reason as the applicant to make the claimed invention. *Ex parte Levengood*, 28 USPQ2d 1300, 1302 (Bd. Pat. App. & Inter. 1993). Further, in response to applicant's argument that the Examiner's conclusion of

obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

Note: The **Appellant's assertions** that the claimed invention has **a circuit (single) further comprising first plurality of internal peripheral and second plurality of external means** along with **three circuit means** for reading, processing and presenting (please see claim 18) **contradicts** with the another **Appellant's assertions** that the figure 2 which is part of the specification of the application under prosecution discloses **an assembly (102)** (not a single circuit as claimed) **further comprising first plurality of internal peripheral and second plurality of external means** along with three circuit means for reading, processing and presenting.

In fact, the claimed invention **does not provide support** on how the **further comprising first plurality of internal peripheral and second plurality of external** along with three circuit means for reading, processing and presenting are **different from each other** and **why and what is that** the same circuit cannot implement limitations of other means. The claimed invention also **do not support on how** the claimed **circuits are different** than the well known circuits including the circuits cited by the references.

The Appellant is trying to accomplish **just** a circuit (e.g., col., 5, lines 11 – 15), which the Ogawa references clearly teaches. The **claimed invention (see claims 19) does not provide the**

benefit of using the internal / external peripherals. The **Appellant did not provide** evidence on **why** the well-known teachings including the cited references are not combinable. The **Appellant did not provide** evidence on **how** the claimed invention is implemented **differently then the well-known teachings** including the cited references.

Thus, the Examiner acknowledges that the initial burden of factually supporting prima facie conclusion of obviousness has been properly meet; the Examiner acknowledges that there is a suggestion or motivation to modify or combine the cited references; the Examiner acknowledges that reasonable expectation of success is demonstrated; the Examiner acknowledges that based on the evidence provided the suggestion to modify and the reasonable expectation success are properly presented and not merely used Appellant's disclosure; the Examiner acknowledges that **a clear and particular showing** of a teaching or motivation to modify Ogawa is properly **established for means comprises a first plurality of the peripheral means internal to the means for processing and a second plurality of the peripheral means external to the means for processing**; the Examiner acknowledges that the motivations **are credited** to the cited references and/or knowledge generally available to one of ordinary skilled in the art; the Examiner acknowledges that the motivations **are to the nature** of the problem to be solved (something needed to perform the processing of the claim); the Examiner acknowledges that the motivations **are based** on objective evidence of record; the Examiner acknowledges that the motivations are **not** merely conclusory statements lacking the required supporting evidence (**please see evidence** abstract, col., 11, lines 58 – 67, lines 27 - 65, col., 9 of the Wilford for additional motivations and advantages of using them).

Thus, wherein the plurality of peripheral means comprises a first plurality of the peripheral means internal to the means for processing and a second plurality of the peripheral means external to the means for processing is clearly understood and based on the presented evidence as taught by the reference and interpreted by the Examiner, these limitations as claimed are indeed not novel and hence the rejection should be maintained.

(12) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the Examiner in the Related Appeals and Interferences section of this Examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

(Note: the Examiner has made an earnest effort to properly address each and every Appellant's arguments of the appeal brief. In any event or reason if more explanation is needed, the Examiner will gladly provide as necessary).

Respectfully submitted,

Haresh Patel

Examiner

Art Unit 2154

July 3, 2006

Conferees:

Follansbee, John (SPE AU 2154)

JOHN FOLLANSBEE
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